1. Introduction

This getting started guide is intended to enable users to set up the Ampere® Altra® Platform Series Mt. Collins Design Validation Test (DVT), Production Validation Test (PVT), and Mass Production (MP) systems and prepare them for use.

1.1. How to Use This Guide

This guide contains numbered procedures that enable you to prepare the Mt. Collins DVT/PVT/MP systems for use.

Note: Going forward, the terms “system,” “server,” “Mt. Collins,” and “Mt. Collins DVT/PVT/MP server” are used interchangeably in this document. Similarly, the terms “CPU,” “SoC,” “host,” and “processor” are used interchangeably in this document, and they refer to the Altra or Altra Max SoC.

1.2. Text Conventions

Table 1 outlines the conventions used to distinguish different types of text in this guide.

Table 1: Text Conventions Used in this Guide

FONT	USAGE
`Consolas Bold`	Typed-in commands, or verbatim user-entered text.
`Consolas`	Text response from the computer.
<text>	Mandatory field.
[text]	Text that may be optionally entered or omitted.
Italic	Variable placeholder.

2. Standard Shipping Configurations

Table 2 lists the standard shipping configuration for the Mt. Collins DVT server.

Table 2: Standard Shipping Configuration for Mt. Collins DVT Server (Sheet 1 of 2)

DEVICE CATEGORY	PART NUMBER	VENDOR	TYPE	CAPACITY	SPEED	QTY	DETAILS
Processor	Altra AC-108021002P[1]	Ampere	–	–	3.00 GHz	2	80 cores supported × 2 sockets
Memory	M393A4K40DB3-CWE	Samsung	RDIMM	16 GB	3200[2]	32	2R × 4, 3200 MT/s
PCIe Network	BCM957504-N425G	Broadcom	NIC	–	–	1	Gen4, x16
NVMe (M.2) SSD	MZ1LB960HAJQ	Samsung	M.2	960 GB	–	1	Gen3, x4[3]
NVMe (U.2) SSD	MZQLB960HAJR	Samsung	U.2	960 GB	–	1	Gen3, x4

Table 2: Standard Shipping Configuration for Mt. Collins DVT Server (Sheet 2 of 2)

DEVICE CATEGORY	PART NUMBER	VENDOR	TYPE	CAPACITY	SPEED	QTY	DETAILS
Operating System	Fedora 39 (version 6.5.6-300.fc39)	Fedora	–	–	–	–	Kernel 6.56

Table 3 lists the standard shipping configuration for the Mt. Collins PVT/MP server.

Table 3: Standard Shipping Configuration for Mt. Collins PVT/MP Server

DEVICE CATEGORY	PART NUMBER	VENDOR	TYPE	CAPACITY	SPEED	QTY	DETAILS
Processor	Altra AC-108021002P[1]	Ampere	–	–	3.00 GHz	2	80 cores supported × 2 sockets
Memory	M393A4K40DB3-CWE	Samsung	RDIMM	16 GB	3200[2]	32	2R × 4, 3200 MT/s
PCIe Network	BCM957504-N425G	Broadcom	NIC	–	–	1	Gen4, x16
NVMe (M.2) SSD	MZ1L2960HCJR	Samsung	M.2	960 GB	–	1	Gen4, x4[4]
NVMe (U.2) SSD	MZQLB960HAJR	Samsung	U.2	960 GB	–	1	Gen3, x4
Operating System	Fedora 39 (version 6.5.6-300.fc39)	Fedora	–	–	–	–	Kernel 6.56

Notes for *Table 2* and *Table 3*:

1. If the system ships with Altra Max, the Part Number is AC-212825002, 128 cores supported × 2 sockets.
2. DDR4 DIMM operating speed is 3200 MT/s.
3. The Mt. Collins DVT server supports only Gen3 PCIe NVMe M.2 SSDs.
4. The Mt. Collins PVT/MP server is shipped with a Gen4 PCIe NVMe M.2 SSD but is backward compatible with Gen3 M.2 SSDs.
5. The VGA port output on the front panel is pixelated on both the DVT and PVT versions. This issue is fixed in the MP version. The VGA port on the rear panel is fully functional on DVT/PVT/MP versions. Refer to *Appendix C: Identifying Mt. Collins Motherboard Revisions (page 36)* for identifying the board revision.

3. Customized Shipping Configuration

If the configuration of the system received differs from the standard shipping configuration listed above, refer to your Sales Order or Packing List for details of the configuration requested by you.

Note that all instructions and steps outlined in this document still apply and are valid for your custom configuration.

4. Minimum Software Requirements

- Fedora 39
- AMI Aptio® V UEFI Firmware
- AMI MegaRAC® BMC Firmware

5. Step 1 — Review the System Contents

1. Open the shipping carton and position the parts on a clean flat surface.
2. Using the list shown in *Table 4*, verify that all parts are in the carton.
3. Visually inspect all parts to ensure that no damage has occurred during shipping.

Table 4: Mt. Collins DVT/PVT/MP Contents List

SERIAL NO.	DESCRIPTION	QUANTITY
1	Mt. Collins DVT/PVT/MP server chassis[2].	1
2	Power cable	2
3	GPU power cable	2
4	BMC Console cable	1
5	Ampere Altra Platform Series Mt. Collins DVT/PVT/MP Getting Started Guide (this document)	1
6	Rail Kit	1

Note:
1. Requires two Ethernet cables and one VGA cable (not included).
2. Refer to *Appendix C: Identifying Mt. Collins Motherboard Revisions (page 36)* for identifying the Mt. Collins motherboard revision.

Figure 1 and *Figure 2* show the rear and front views, respectively, of the Mt. Collins servers along with the PCIe resource assignments, available ports, and buttons.

Figure 1: Rear View Showing the PCIe Resource Assignments for the Mt. Collins Server

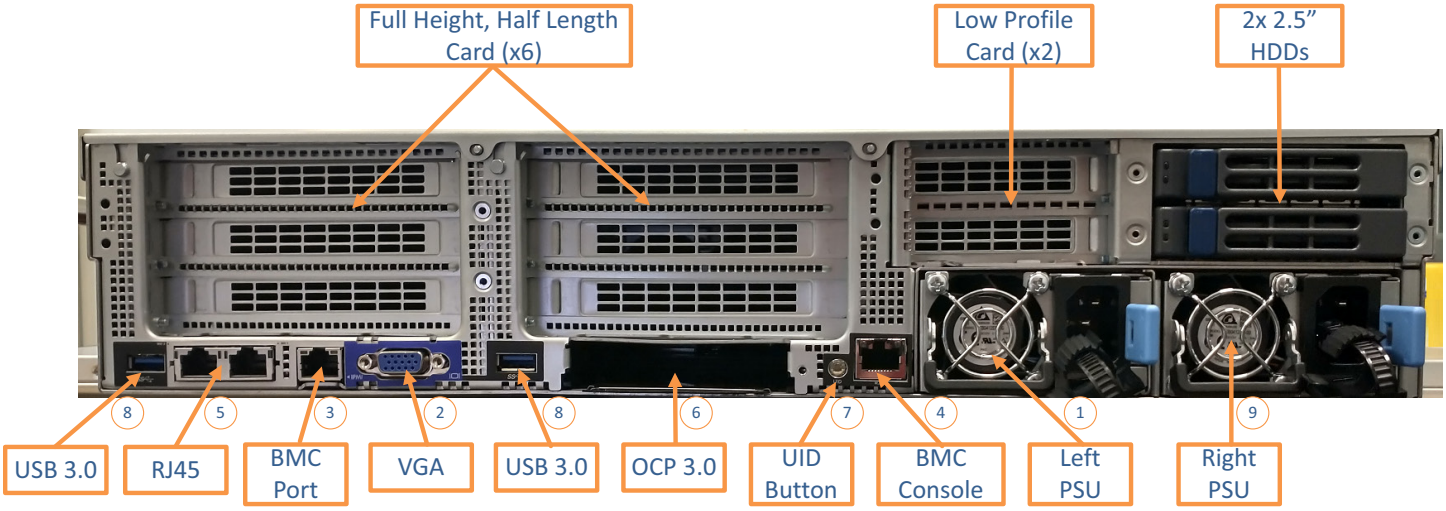


Table 5 lists the descriptions for the buttons, ports, and connectors highlighted in Figure 1, along with their functional status.

Table 5: Ports, Connectors, and Buttons on the Rear Side of the Mt. Collins Server

NO.	DESCRIPTION	FUNCTIONAL STATUS
1	Left Power Supply Unit (PSU)	Functional
2	Rear VGA Connector	Functional
3	BMC Ethernet Port	Functional
4	BMC Console Connector (Serial Over RJ45)	Functional
5	2x 1G CPU Ethernet Port	Functional
6	OCP 3.0	Functional
7	UID Button	Functional
8	2x USB Ports	Functional
9	Right Power Supply Unit (PSU)	Functional
10	1x PCIe M.2 NVMe SSD on Motherboard[1]	Functional

Note:
1. Mt. Collins has one M.2 NVMe SSD slot available on the motherboard.

Figure 2 shows the front view of the Mt. Collins server.

Figure 2: Front View of the Mt. Collins Server

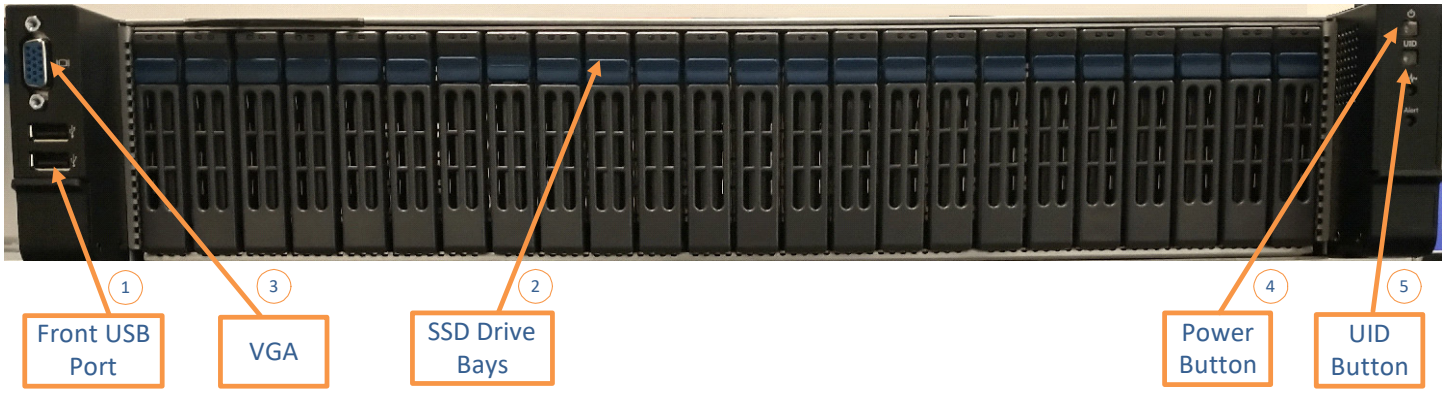


Table 6 lists the descriptions for the buttons, ports, connectors, and drive bays highlighted in Figure 2, along with their functional status.

Table 6: Ports, Connectors, and Buttons on the Front Side of the Mt. Collins Server

NO.	DESCRIPTION	FUNCTIONAL STATUS
1	Front Panel USB Port	Functional
2	24x 2.5” NVMe SSD Drive Bays	Functional
3	Front VGA Connector[1]	Functional
4	Power Button	Functional
5	UID	Functional

Note:
1. On the Mt. Collins DVT/PVT versions, the VGA port output on the front panel is pixelated. This issue is fixed on the Mt. Collins MP version and the VGA port on the front panel is fully functional.

5.1. PCIe Slots’ Resource Availability

Figure 3 shows the default PCIe resources configured on the riser cages of a Mt. Collins server.

Figure 3: PCIe Slots’ Resource Availability on the Mt. Collins Server

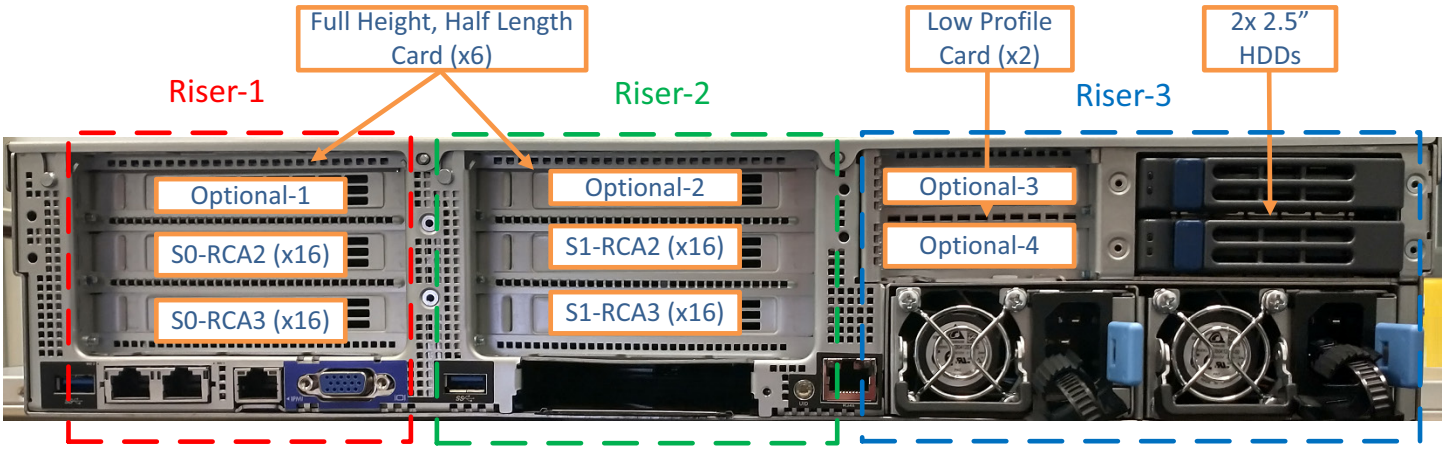


Figure 4 shows the different Riser combinations without additional drives on Riser-3.

Figure 4: Riser Combinations Without Additional Drives on Riser-3

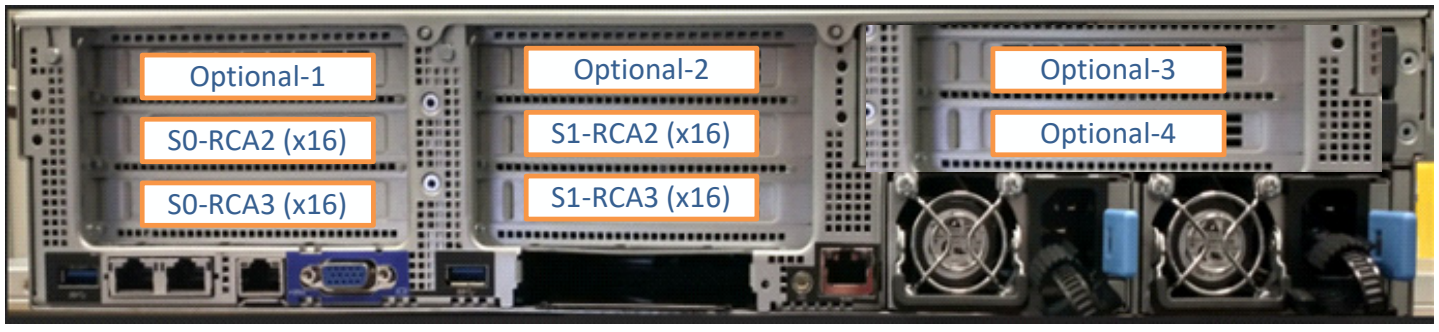


Table 7: PCIe Ports on Mt. Collins Server

NO.	PCIE PORT#		RISER#	AVAILABLE ON 2S2P	AVAILABLE ON 2S1P
	ALTRA	ALTRA MAX			
1	S0 – RCA3 x16	S0 – RCA3 x16	Riser 1	Yes	Yes
2	S0 – RCA2 x16	S0 – RCA2 x16	Riser 1	Yes	Yes
3	Optional-1[1] x8 J84-MB <->J81-R S0-RCB2B[2]	Optional-1[1] x16 J84-MB <->J81-R S0-RCA7A[2] J85-MB <->J82-R S0-RCA7B[2]	Riser 1	Yes	Yes
4	S1 – RCA3 x16	S1 – RCA3 x16	Riser 2	Yes	No
5	S1 – RCA2 x16	S1 – RCA2 x16	Riser 2	Yes	No
6	Optional-2[1] x8 J83-MB <->J82-R S1-RCB0A[2]	Optional-2[1] x16 J83-MB <->J82-R S1-RCA4A[2] J90-MB <->J81-R S1-RCA4B[2]	Riser 2	Yes	No
7	Optional-3[1] x8 J86-MB <->J86-R S1-RCB0B[2]	Optional-3[1] x16 J86-MB <->J86-R S1-RCA5A[2] J89-MB <->J89-R S1-RCA5B[2]	Riser 3	Yes	No
8	Optional-4[1] x8 J87-MB <->J87-R S1-RCB2A[2]	Optional-4[1] x16 J87-MB <->J87-R S1-RCA6A[2] J88-MB <->J88-R S1-RCA6B[2]	Riser 3	Yes	No

1. This is an optional slot. To make this slot work in x16 mode, two of the sliver connectors going to the front panel NVMe backplane must be removed and routed to the sliver PCIe connectors on the riser card.
2. Slim SAS Cable routing from connector JXX-MB (motherboard) to JXX-R (riser cage).

Figure 5 shows the default PCIe resource distribution for the front panel NVMe drives on an Altra based Mt. Collins Server.

Figure 5: PCIe Slots Resource Distribution for the Front Panel NVMe Drives on an Altra Based Mt. Collins Server

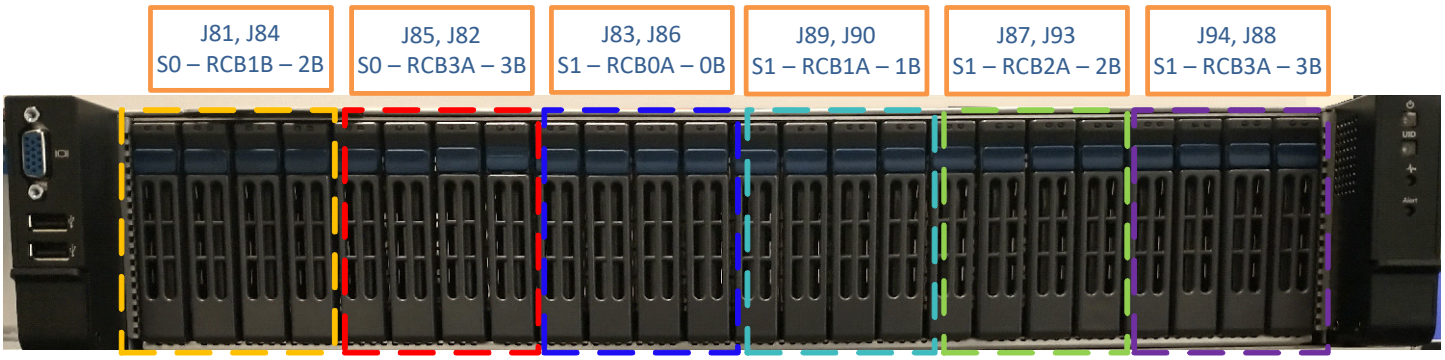


Table 8 lists the NVMe PCIe resource availability for an Altra based Mt. Collins Server. The Altra Max configuration in Table 8 is when Altra is replaced with Altra Max in an Altra based Mt. Collins Server without changing the slim cables in the chassis.

Table 8: NVMe PCIe Resource Availability for Altra Based Mt. Collins Server

NO.	CONNECTOR	PCIE PORT#		SLOT RANGE	DRIVE MAPPING UNDER OS		AVAILABLE ON 2S2P	AVAILABLE ON 2S1P
		ALTRA	ALTRA MAX		ALTRA	ALTRA MAX		
1	M.2	S0 – RCB0A	S0 – RCA4B	NA	NVMe 0	NVMe 2	Yes	Yes
2	J81	S0 – RCB1B	S0 – RCA4A	0-1	NVMe 1-2	NVMe 0-1	Yes	Yes
3	J84	S0 – RCB2B	S0 – RCA7A	2-3	NVMe 3-4	NVMe 5-6	Yes	Yes
4	J85	S0 – RCB3A	S0 – RCA7B	4-5	NVMe 5-6	NVMe 7-8	Yes	Yes
5	J82	S0 – RCB3B	S0 – RCA6B	6-7	NVMe 7-8	NVMe 3-4	Yes	Yes
6	J83	S1 – RCB0A	S1 – RCA4B	8-9	NVMe 9-10	NVMe 11-12	Yes	No
7	J86	S1 – RCB0B	S1 – RCA5B	10-11	NVMe 11-12	NVMe 15-16	Yes	No
8	J89	S1 – RCB1A	S1 – RCA5A	12-13	NVMe 13-14	NVMe 13-14	Yes	No
9	J90	S1 – RCB1B	S1 – RCA4A	14-15	NVMe 15-16	NVMe 9-10	Yes	No
10	J87	S1 – RCB2A	S1 – RCA6A	16-17	NVMe 17-18	NVMe 17-18	Yes	No
11	J93	S1 – RCB2B	S1 – RCA7A	18-19	NVMe 19-20	NVMe 21-22	Yes	No
12	J94	S1 – RCB3A	S1 – RCA7B	20-21	NVMe 21-22	NVMe 23-24	Yes	No
13	J88	S1 – RCB3B	S1 – RCA6B	22-23	NVMe 23-24	NVMe 19-20	Yes	No

Figure 6 shows the default PCIe resource distribution for the front panel NVMe drives on an Altra Max based Mt Collins Server.

Figure 6: PCIe Slots Resource Distribution for the Front Panel NVMe Drives on an Altra Max Based Mt. Collins Server

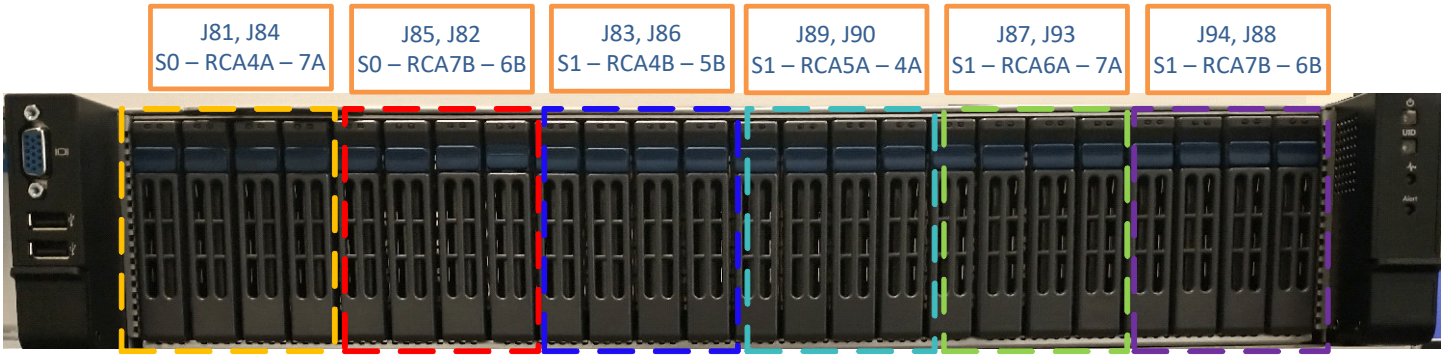


Table 9 lists the NVMe PCIe resource availability for an Altra Max based Mt. Collins Server. The Altra configuration in *Table 9* is when Altra Max is replaced with Altra in an Altra Max based Mt. Collins Server without changing the slim cables in the chassis.

Table 9: NVMe PCIe Resource Availability for Altra Max Based Mt. Collins Server

NO.	CONNECTOR	PCIE PORT#		SLOT RANGE	DRIVE MAPPING UNDER OS		AVAILABLE ON 2S2P	AVAILABLE ON 2S1P
		ALTRA MAX	ALTRA		ALTRA MAX	ALTRA		
1	M.2	S0 – RCA4B	S0- RCB0A	NA	NVMe 2	NVMe 0	Yes	Yes
2	J81	S0 – RCA4A	S0 – RCB1B	0-1	NVMe 0-1	NVMe 1-2	Yes	Yes
3	J84	S0 – RCA6B	S0 – RCB3B	2-3	NVMe 3-4	NVMe 7-8	Yes	Yes
4	J85	S0 – RCA7A	S0 – RCB2B	4-5	NVMe 5-6	NVMe 3-4	Yes	Yes
5	J82	S0 – RCA7B	S0 – RCB3A	6-7	NVMe 7-8	NVMe 5-6	Yes	Yes
6	J83	S1 – RCA4A	S1 – RCB1B	8-9	NVMe 9-10	NVMe 15-16	Yes	No
7	J86	S1 – RCA4B	S1 – RCB0A	10-11	NVMe 11-12	NVMe 9-10	Yes	No
8	J89	S1 – RCA5A	S1 – RCB1A	12-13	NVMe 13-14	NVMe 13-14	Yes	No
9	J90	S1 – RCA5B	S1 – RCB0B	14-15	NVMe 15-16	NVMe 11-12	Yes	No
10	J87	S1 – RCA6A	S1 – RCB2A	16-17	NVMe 17-18	NVMe 17-18	Yes	No
11	J93	S1 – RCA6B	S1 – RCB3B	18-19	NVMe 19-20	NVMe 23-24	Yes	No
12	J94	S1 – RCA7A	S1 – RCB2B	20-21	NVMe 21-22	NVMe 19-20	Yes	No
13	J88	S1 – RCA7B	S1 – RCB3A	22-23	NVMe 23-24	NVMe 21-22	Yes	No

Figure 7 shows the block diagram of the Mt. Collins server.

Figure 7: Mt. Collins Server Block Diagram

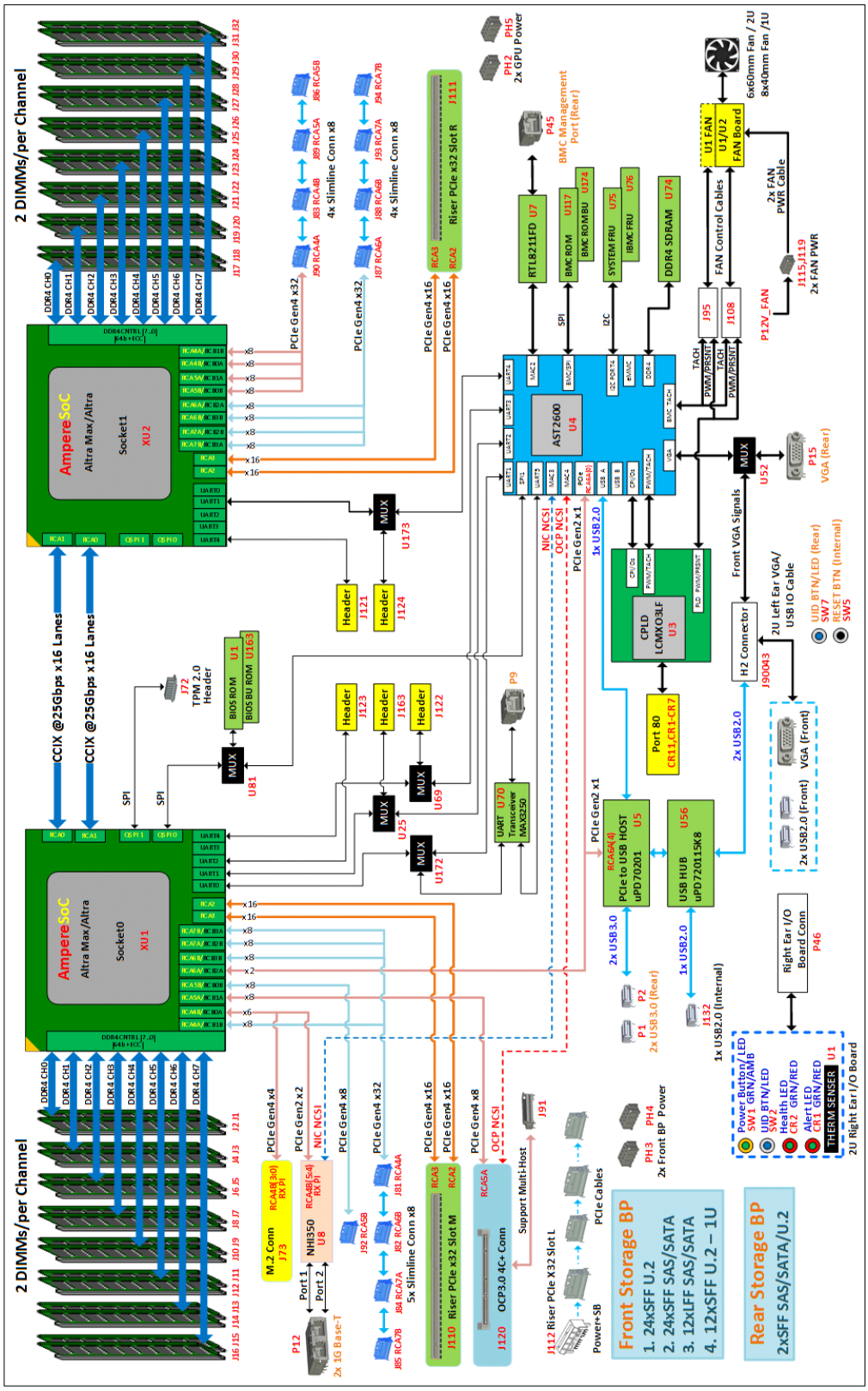


Figure 8 shows the Mt. Collins DVT/PVT/MP server's memory topology with two DIMMs per channel (2DPC).

Figure 8: Mt. Collins DVT/PVT/MP Server Memory Topology with 2DPC

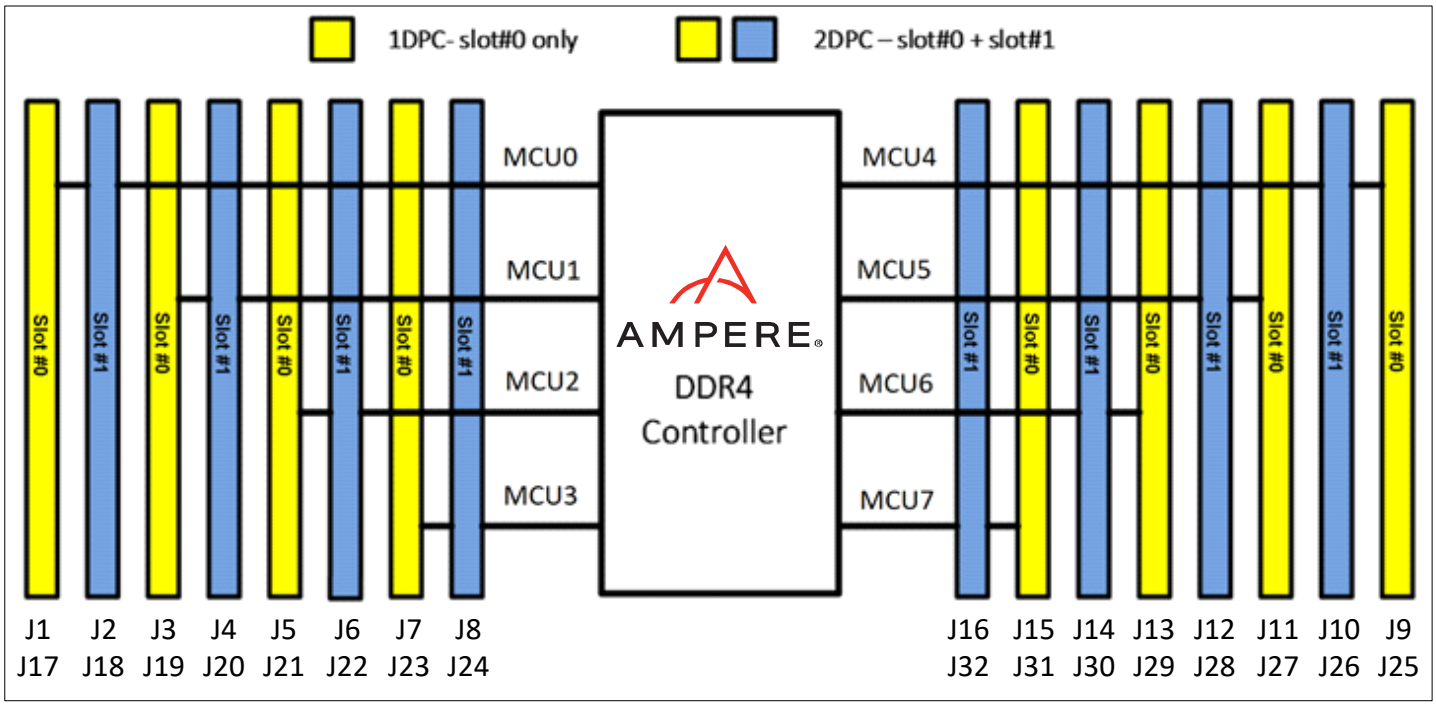


Table 10 lists the memory channel configurations supported on the Mt. Collins DVT/PVT/MP server.

Table 10: Memory Channel Configurations Supported on Mt. Collins DVT/PVT/MP Server

NUMBER OF CHANNELS	CHANNELS USED							
	MCU0	MCU1	MCU2	MCU3	MCU4	MCU5	MCU6	MCU7
	0	1	2	3	4	5	6	7
1	Y	—	—	—	—	—	—	—
1	—	—	—	—	Y	—	—	—
2	Y	—	—	—	Y	—	—	—
4	Y	Y	—	—	Y	Y	—	—
6	Y	Y	Y		Y	Y	Y	
8	Y	Y	Y	Y	Y	Y	Y	Y

Each socket on Mt. Collins must comply with the installations listed in *Table 10*, but memory on the Socket 0 channels is not required to be the same size as the memory on the Socket 1 channels. However, DIMM modules on all channels on a socket must be identically sized.

Table 11 lists the Mt. Collins DVT/PVT/MP server's DDR memory population table.

Table 11: Mt. Collins DDR4 Memory Population Table (Max 32 DIMM Slots)

MT. COLLINS DDR4 MEMORY POPULATION TABLE (MAX 32 DIMM SLOTS)	
DIMM COUNTS	**MEMORY POPULATION SEQUENCE**
2 SoCs and 2 DIMMs	J1/J17
2 SoCs and 4 DIMMs	J1/J9/J17/J25
2 SoCs and 8 DIMMs	J1/J3/J9/J11/J17/J19/J25/J27
2 SoCs and 16 DIMMs	J1/J3/J5/J7/J9/J11/J13/J15/J17/J19/J21/J23/J25/J27/J29/J31
2 SoCs and 32 DIMMs	J1/J2/J3/J4/J5/J6/J7/J8/J9/J10/J11/J12/J13/J14/J15/J16/J17/J18/J19/J20/J21/J22/J23/J24/J25/J26/J27/J28/J29/J30/J31

Figure 9 shows the Mt. Collins DVT/PVT/MP server's memory topology with 2DPC.

Figure 9: Mt. Collins DVT/PVT/MP Memory Topology with 2DPC

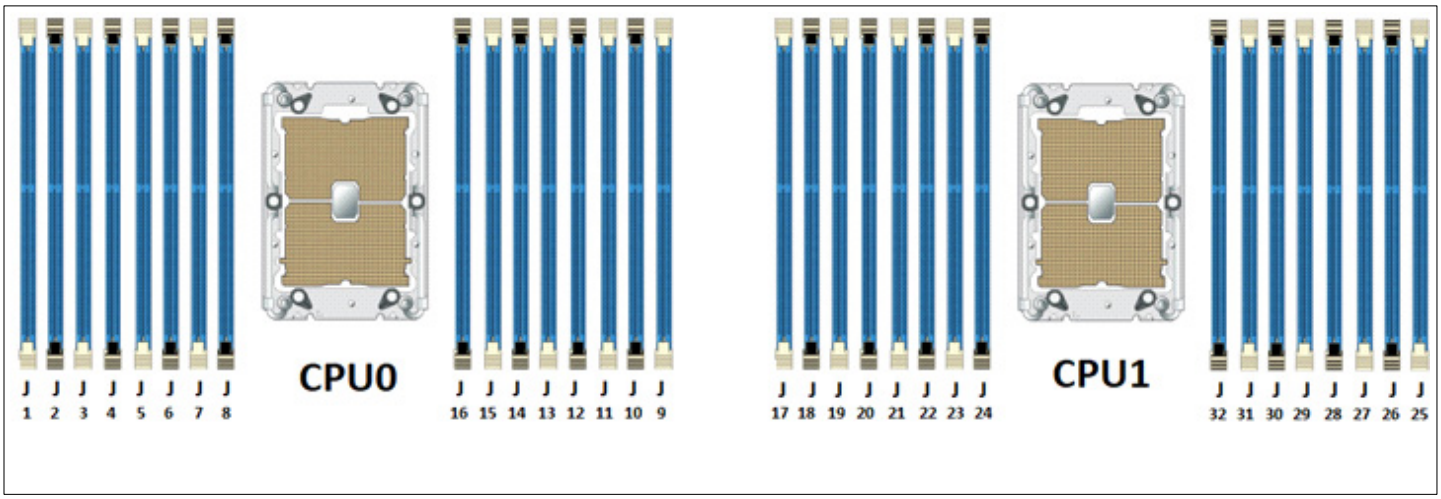


Table 12 and *Table 13* list the memory channel configurations supported on the Mt. Collins DVT/PVT/MP server for Socket0 and Socket1, respectively.

Table 12: Mt. Collins DVT/PVT/MP Server Supported Memory Channel Configurations – Socket0

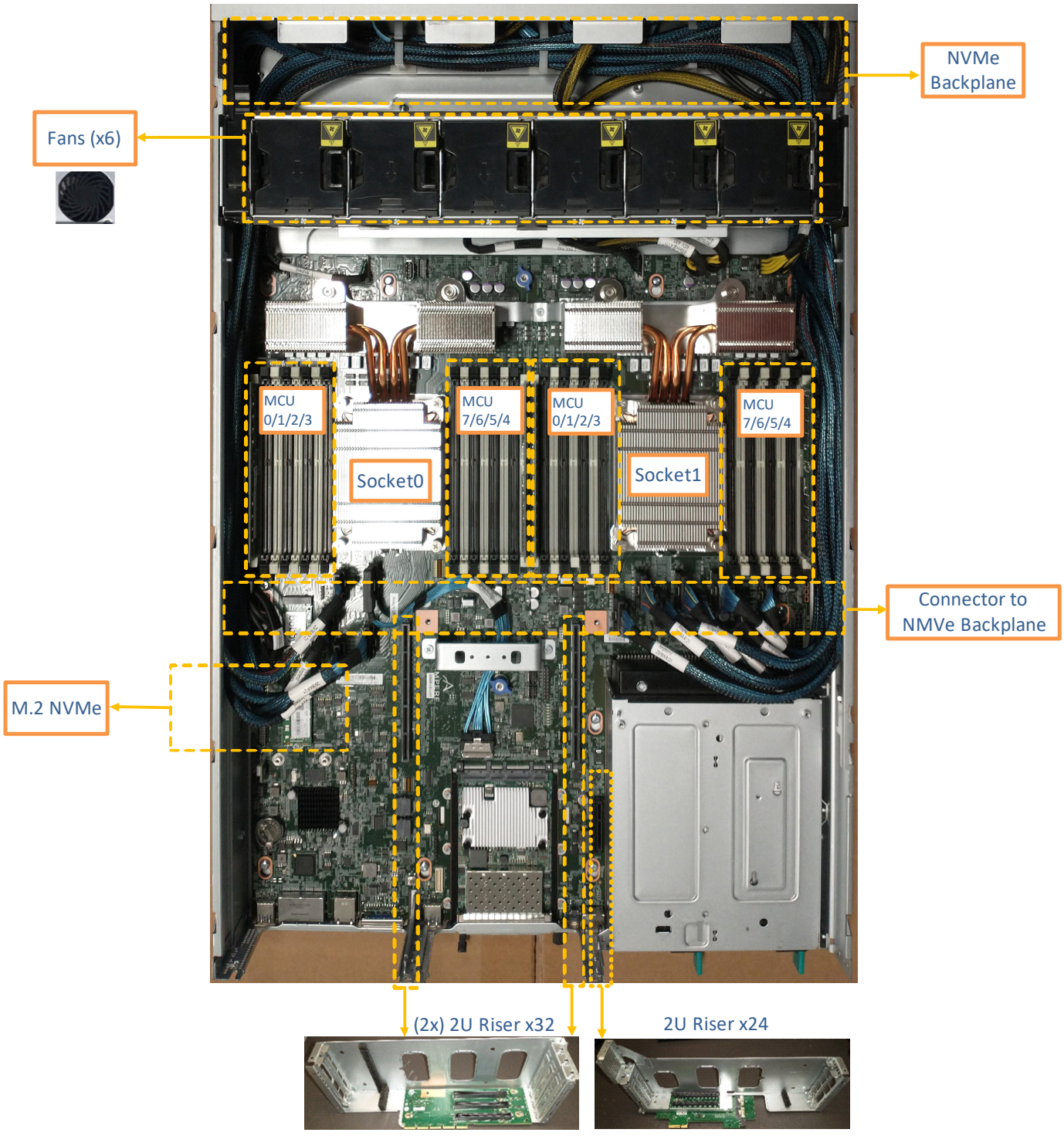
CONFIGURATION	DIMM SOCKETS POPULATED															
	SOCKET0 – MCUs AND DIMM SLOTS															
	MCU0		MCU1		MCU2		MCU3		MCU7		MCU6		MCU5		MCU4	
	#1	#2	#3	#4	#5	#6	#7	#8	#16	#15	#14	#13	#12	#11	#10	#9
2S2P	Y	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
2S2P	Y	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Y
2S2P	Y	–	Y	–	–	–	–	–	–	–	–	–	–	Y	–	Y
2S2P	Y	–	Y	–	Y	–	Y	–	–	Y	–	Y	–	Y	–	Y
2S2P	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Table 13: Mt. Collins DVT/PVT/MP Server Supported Memory Channel Configurations – Socket1

CONFIGURATION	DIMM SOCKETS POPULATED															
	SOCKET1 – MCUs AND DIMM SLOTS															
	MCU0		MCU1		MCU2		MCU3		MCU7		MCU6		MCU5		MCU4	
	#17	#18	#19	#20	#21	#22	#23	#24	#32	#31	#30	#29	#28	#27	#26	#25
2S2P	Y	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–
2S2P	Y	–	–	–	–	–	–	–	–	–	–	–	–	–	–	Y
2S2P	Y	–	Y	–	–	–	–	–	–	–	–	–	–	Y	–	Y
2S2P	Y	–	Y	–	Y	–	Y	–	–	Y	–	Y	–	Y	–	Y
2S2P	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y

Figure 10 shows the 2S Mt. Collins server with the top cover of the chassis removed.

Figure 10: Mt. Collins Server with the Top Cover Removed



Note: The Ampere Altra/Altra Max SoC is installed into the socket with specific installation procedures that include certain torque settings to ensure proper pin contact, thermal contact, and safety of the socket pins. To avoid issues, do not try to remove the heat sink and SoC, unless you are adequately trained to do so.

6. Step 2 — Equipment Required

Table 14 lists the equipment required to set up the Mt. Collins server as per the instructions provided in this document.

Table 14: Equipment Required to Set up the Mt. Collins Server

#	ITEM	TYPE/MODEL	QTY	SAMPLE PICTURE
1	Mt. Collins server	Mt. Collins DVT/PVT/MP motherboard installed in the chassis	1	
2	Ethernet cable	RJ45 Ethernet cable	2	
3	BMC console terminal	RJ-45 to USB-A	1	
4	System (PC or laptop)	Ubuntu Linux PC or Laptop	1	
5	Network hub/switch	1/10 GbE network hub/switch	1	
6	VGA cable	VGA connector cable	1	
7	Monitor	VGA monitor	1	
8	Power cable	Power cable	2	

7. Step 3 — Bring Up the System

This section describes how to power up and initialize the Mt. Collins server.

1. Before powering up the Mt. Collins server, connect the VGA cable from the rear VGA port on the Mt. Collins server to the VGA port on the display monitor. The BMC IP address will be displayed on the VGA monitor once the system is powered up.
2. Connect the two power cables to the Mt. Collins server and then to the appropriate power sources.
3. Connect an RJ45 Ethernet cable from the BMC Ethernet Management port of the Mt. Collins server to the network switch which provides a DHCP IP address.
4. If Ethernet connectivity is needed for the host Linux system, connect an RJ45 cable to the CPU 1G Ethernet port.

7.1. Step 3a — BMC Console Connectivity

5. On a Linux PC terminal, issue the command `minicom -D /dev/ttyUSB0 -b 115200` to establish BMC console connectivity (where `ttyUSB0` is the assigned USB Serial port for BMC).

Note: It may be necessary to turn off hardware/software flow control in minicom for certain serial-to-USB cables to function properly.

7.2. Step 3b — Powering on Mt. Collins Server

6. Connect the power cable to the Mt. Collins server and then to the appropriate power source.
7. The system is pre-loaded with Fedora 39. After powering up the system, the CPU first boots AMI UEFI BIOS and then loads the installed operating system. To access the BIOS menu, the user must press either the “Esc” or “Del” keys at the beginning of the boot process. Otherwise, the system will automatically boot the CentOS operating system based on the pre-configured options.

Note:

- The default login ID for Fedora is “root” and the default login password for Fedora is “root”.
- The Mt. Collins DVT/PVT/MP system (Linux) console can be accessed through IPMI SOL using `ipmitool` from any Linux terminal that has network connectivity to the BMC IP address (user name: “admin”; password: “admin”).

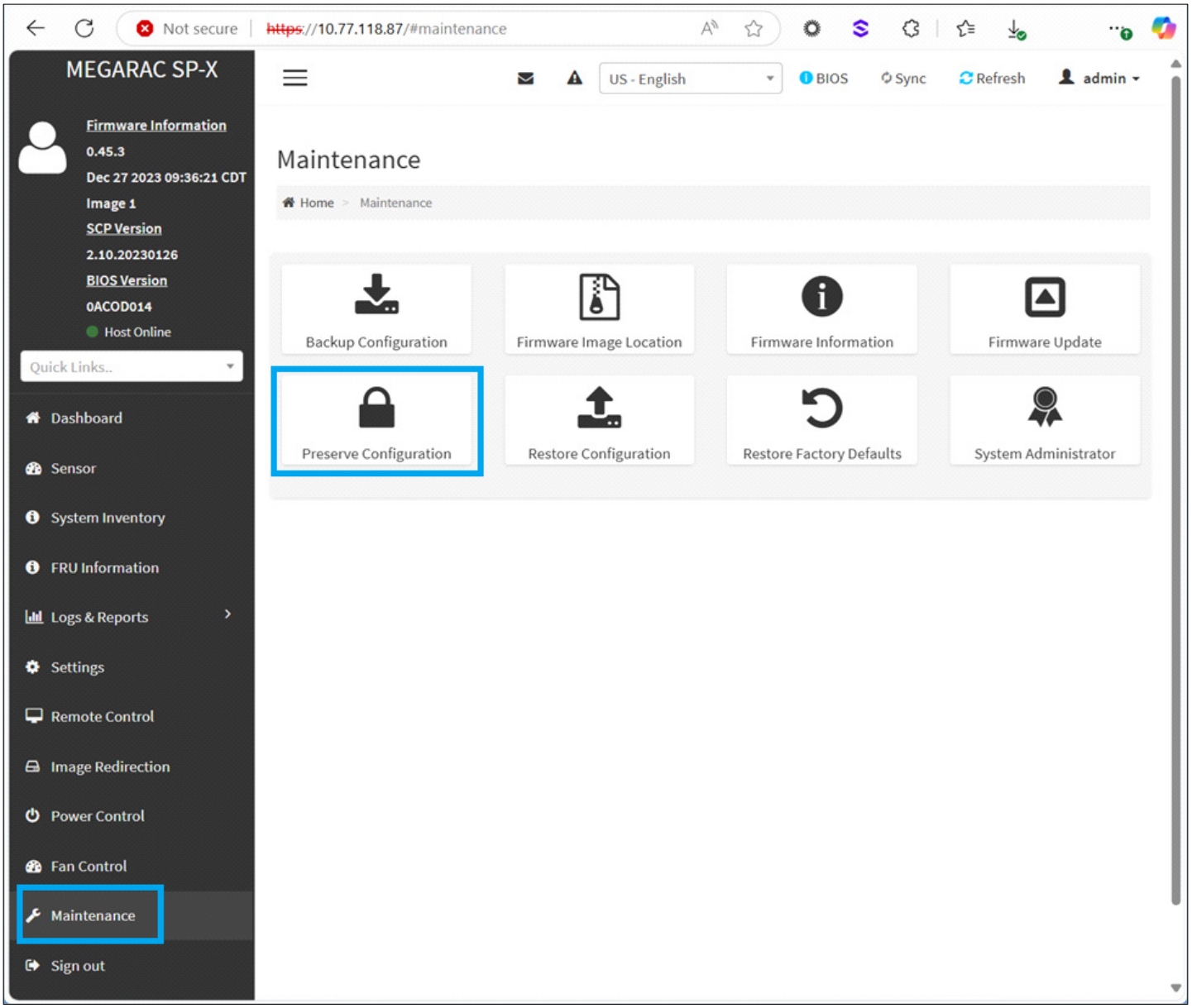
  `ipmitool -I lanplus -H <BMC IP address> -U admin -P admin sol activate`

8. Step 4 — Upgrade BMC Firmware

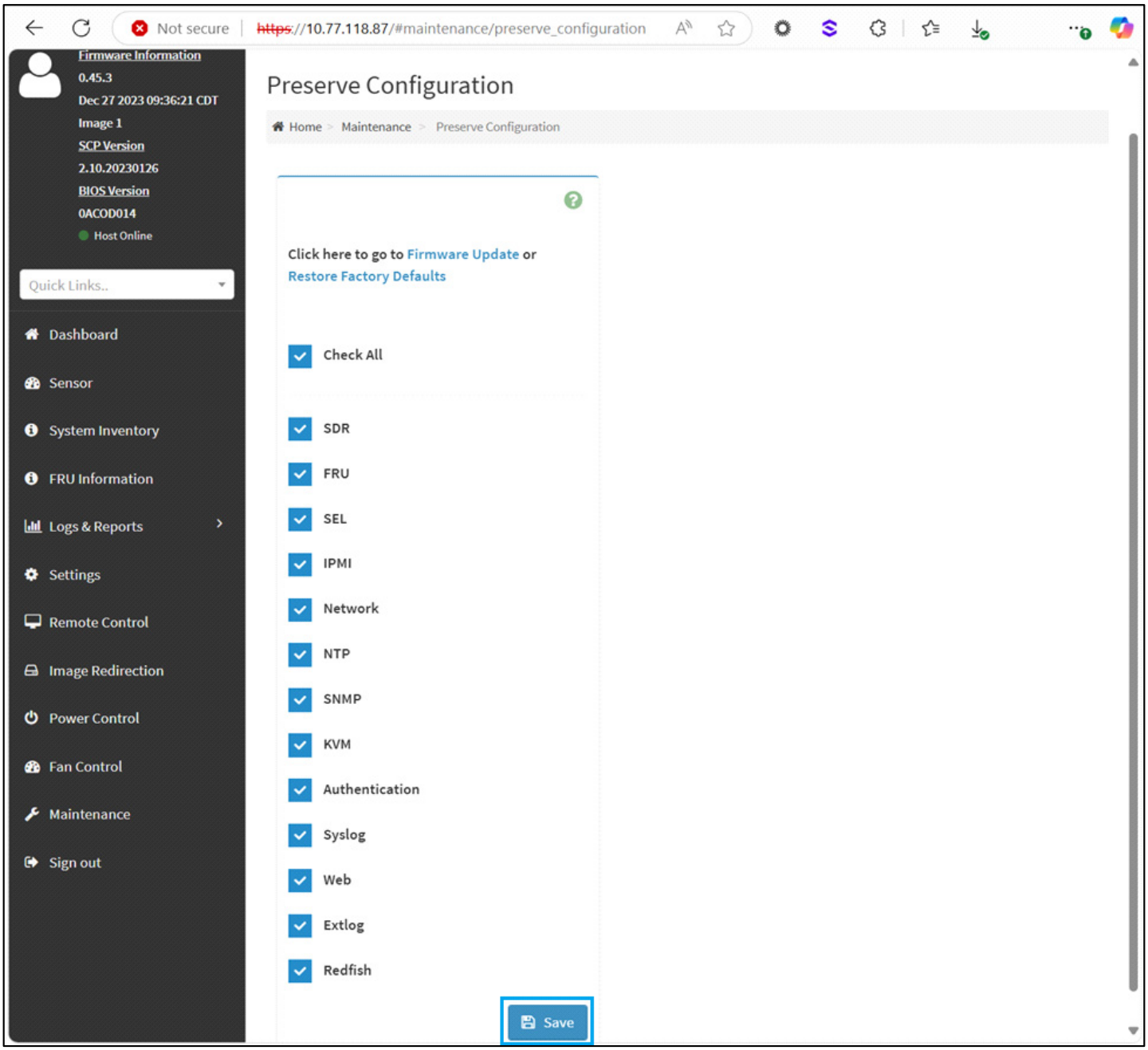
8.1. Step 4a — Preserving Existing BMC Configuration

To preserve the previous BMC configuration after a BMC firmware upgrade, follow these steps.

1. Launch a Web browser (such as Firefox or Chrome) and type **https://BMC_IP** in the address field to access the BMC WebUI.
   Note: The login ID for BMC is “admin”, and the login password is “admin”.
2. Click Maintenance > Preserve Configuration.



3. Select the configurations that you wish to preserve and click **Save**.



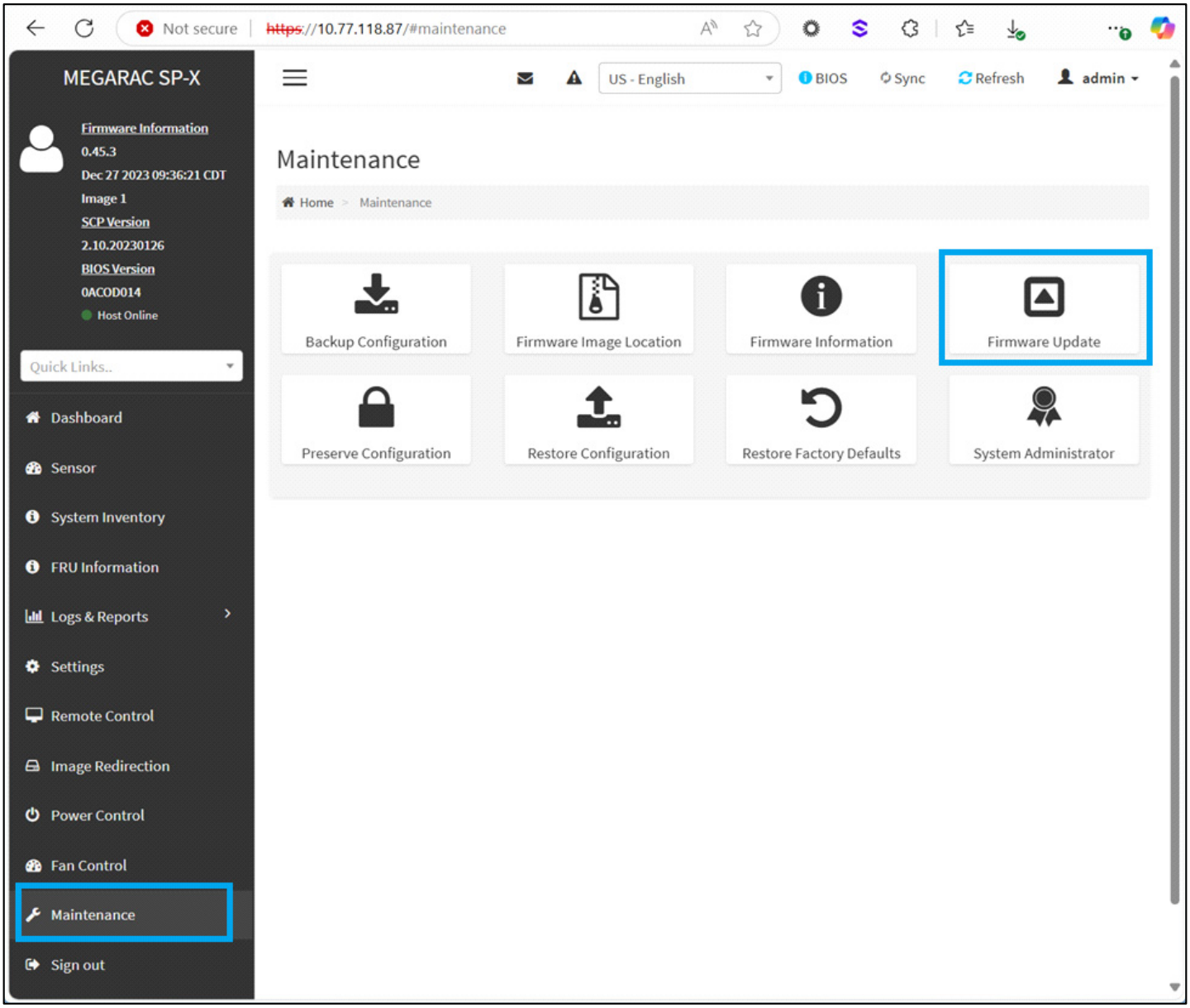
Step 4b — Upgrade BMC Firmware Using WebUI

The BMC firmware can be upgraded through WebUI by following these steps.

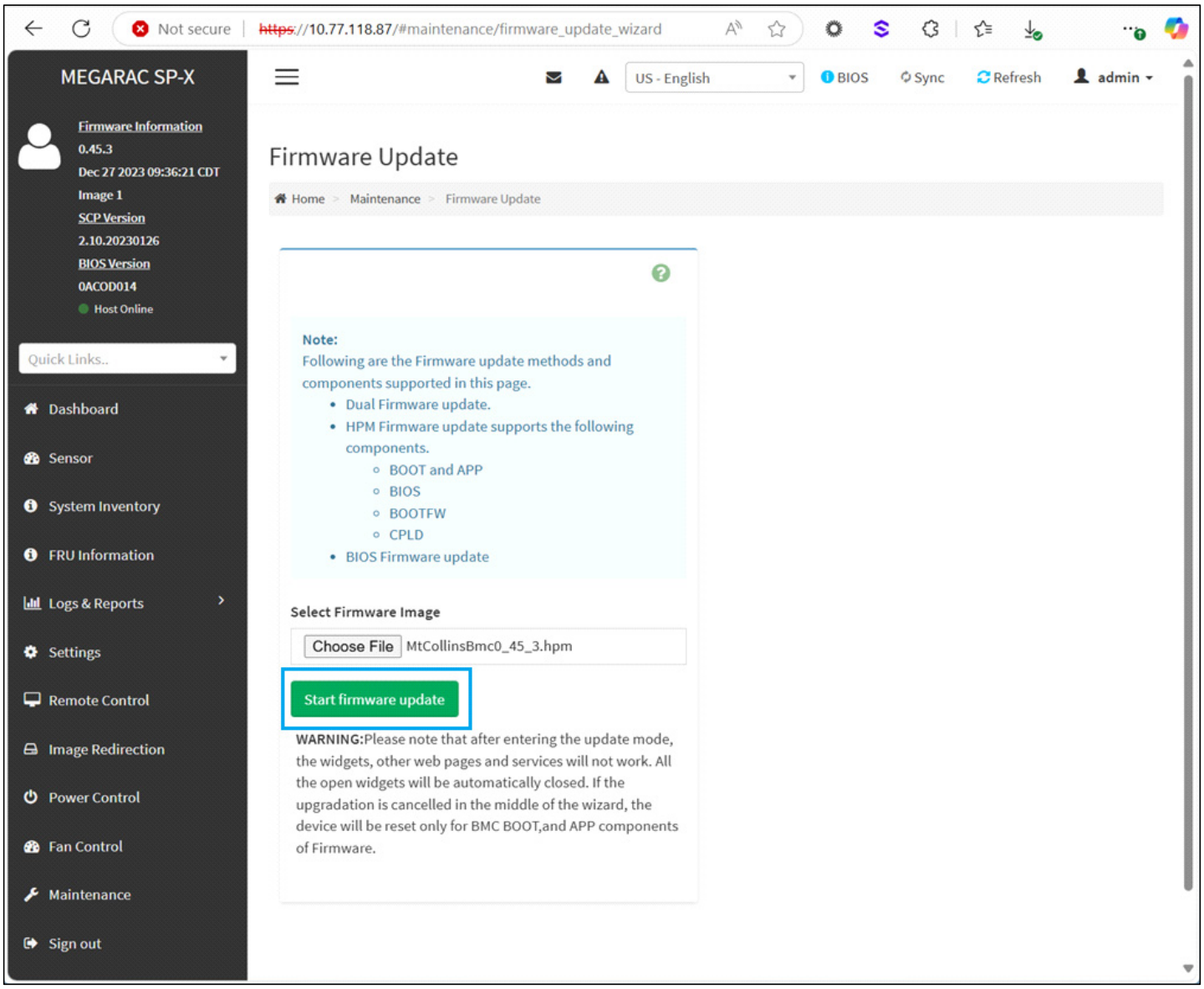
1. Launch a Web browser (such as Firefox or Chrome) and type **https://BMC_IP** in the address field to access the BMC WebUI.

   Note: The login ID for BMC is “admin”, and the login password is “admin”.

2. Click Maintenance > Firmware Update.

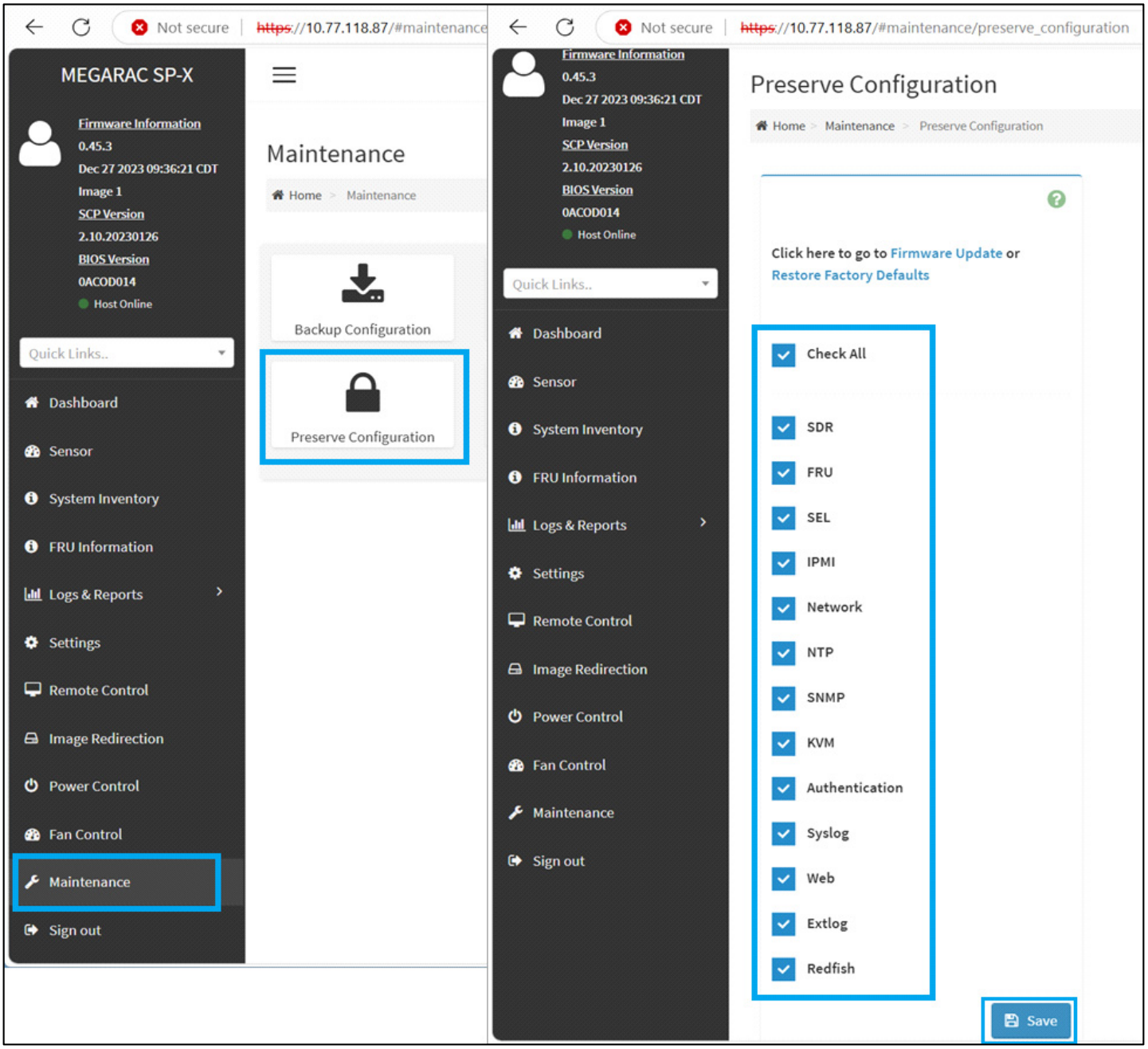


3. Select the BMC firmware image file (HPM or IMA format).



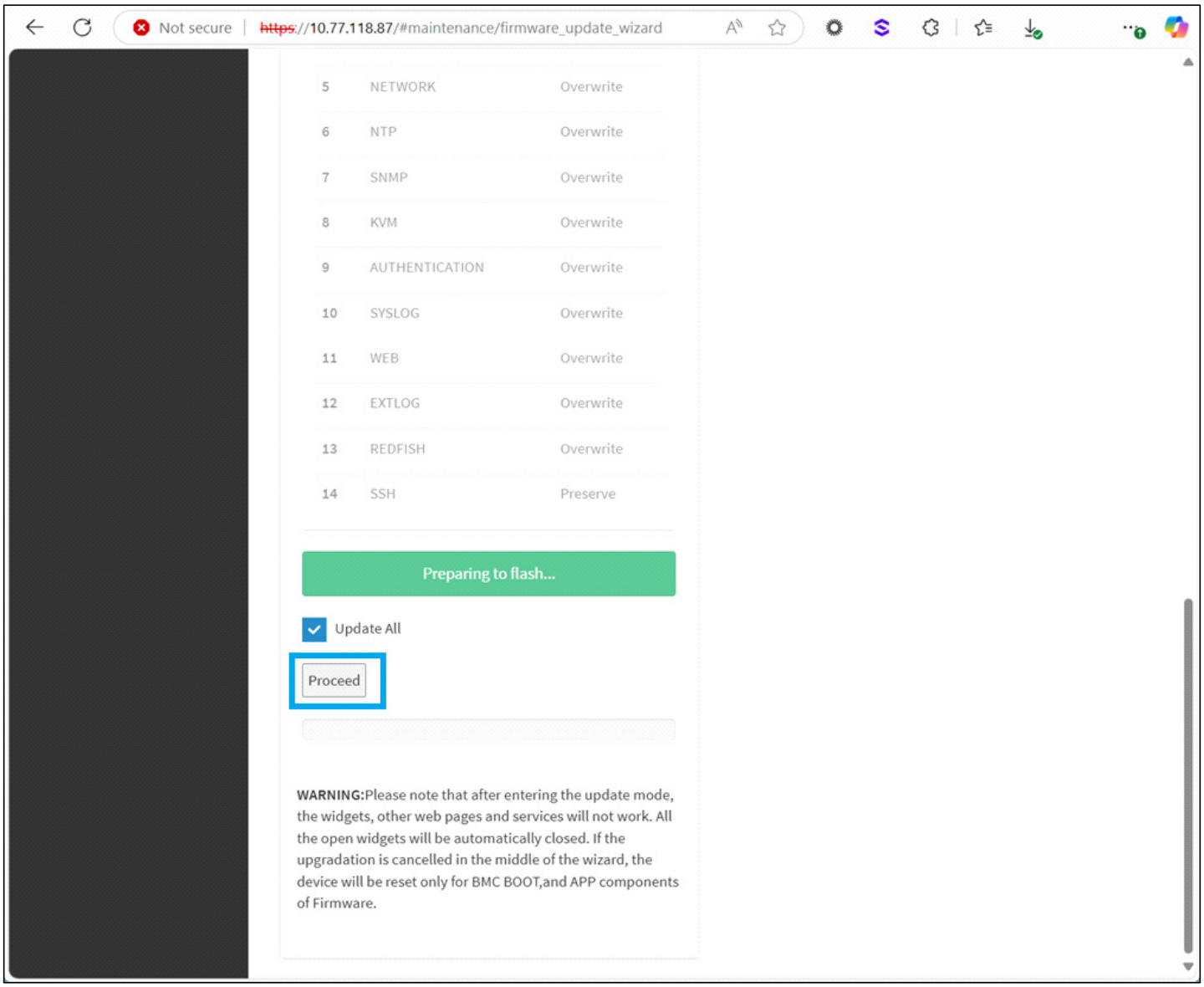
Before clicking **Start firmware update**, if there is a requirement for the existing BMC configuration to be restored after upgrading the BMC firmware, then select the **Preserve all configuration** check-box.

Preserving the existing BMC configuration can also be enabled from **Maintenance > Preserve Configuration**. Check the configuration items that need to be preserved and restored after the firmware upgrade.

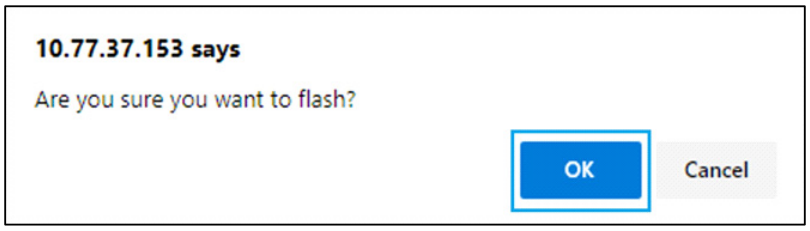


4. After the **Preserve Configuration** items are selected, click **Start firmware upgrade.**

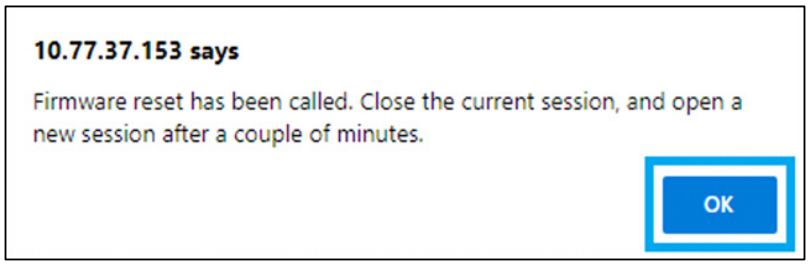
5. Check the component versions. If the versions differ, click **Proceed** to start the upgrade.



6. Click OK to start the firmware upgrade process.



7. After the upgrade is complete, the following dialog box is displayed. Click OK.



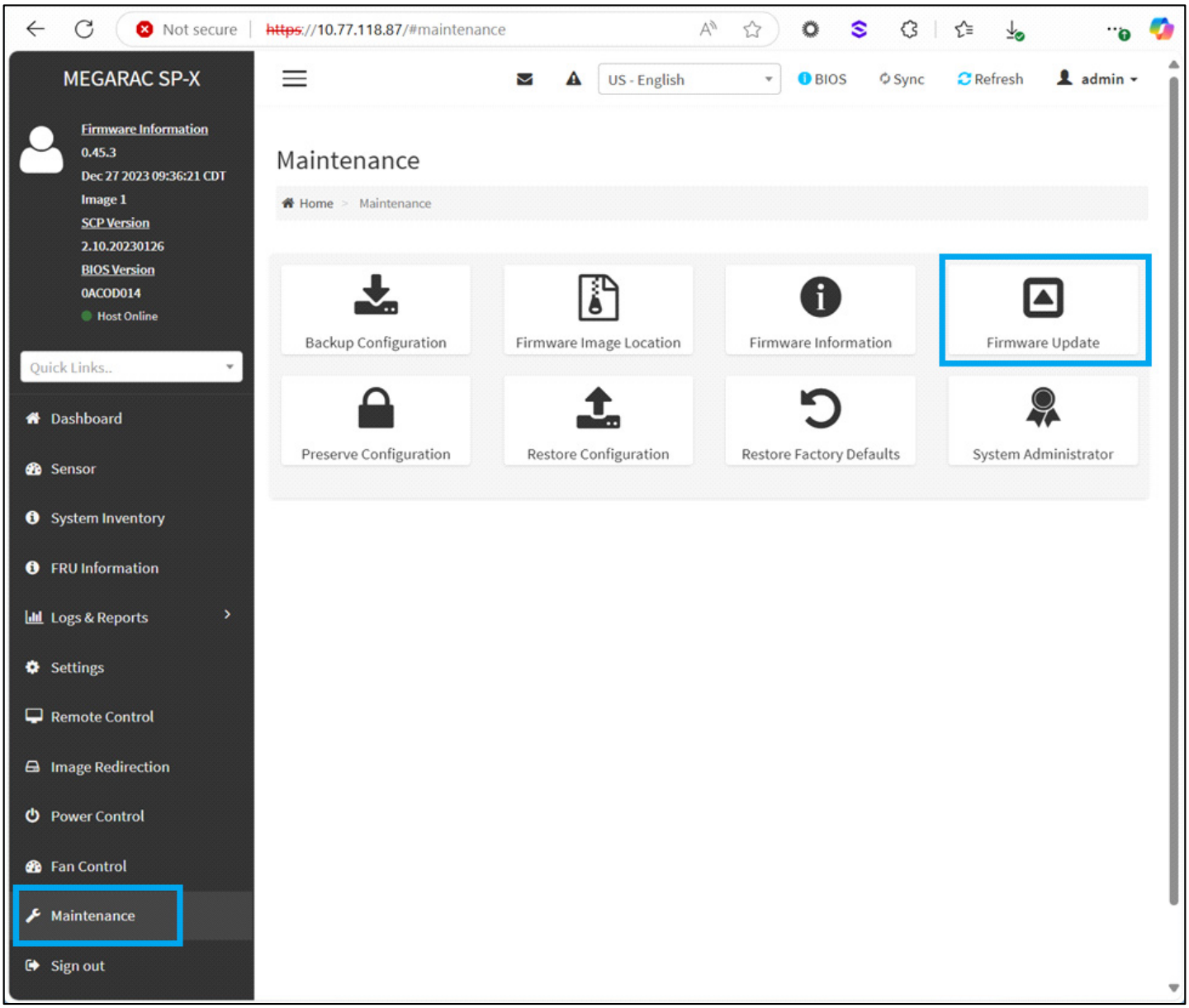
9. Step 5 — Upgrade SCP Firmware

The SCP firmware can be upgraded using either WebUI or IPMI as described in the following sections.

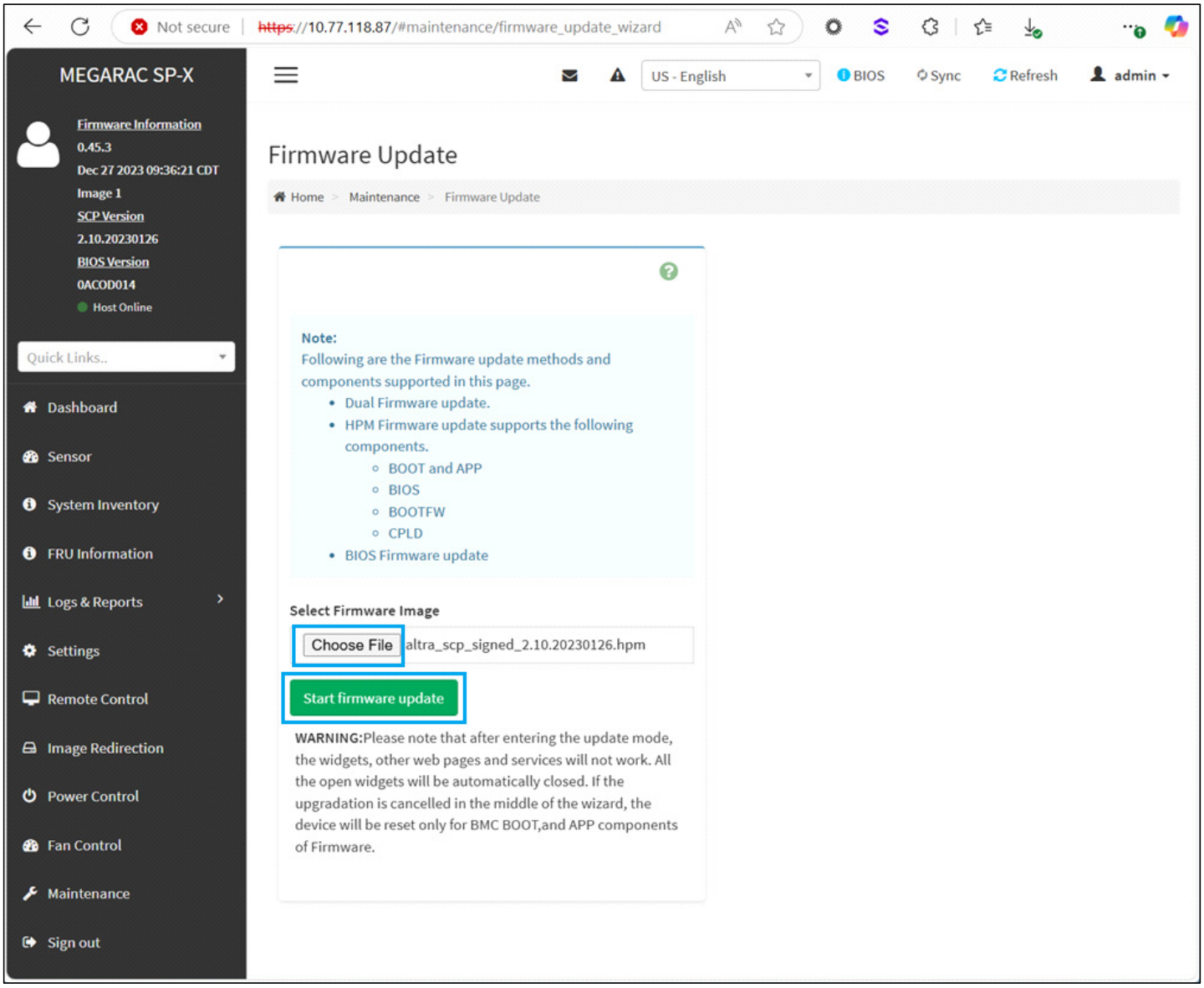
9.1. Step 5a — Upgrade SCP Firmware Using WebUI

The SCP firmware can be upgraded using WebUI by following the steps listed below.

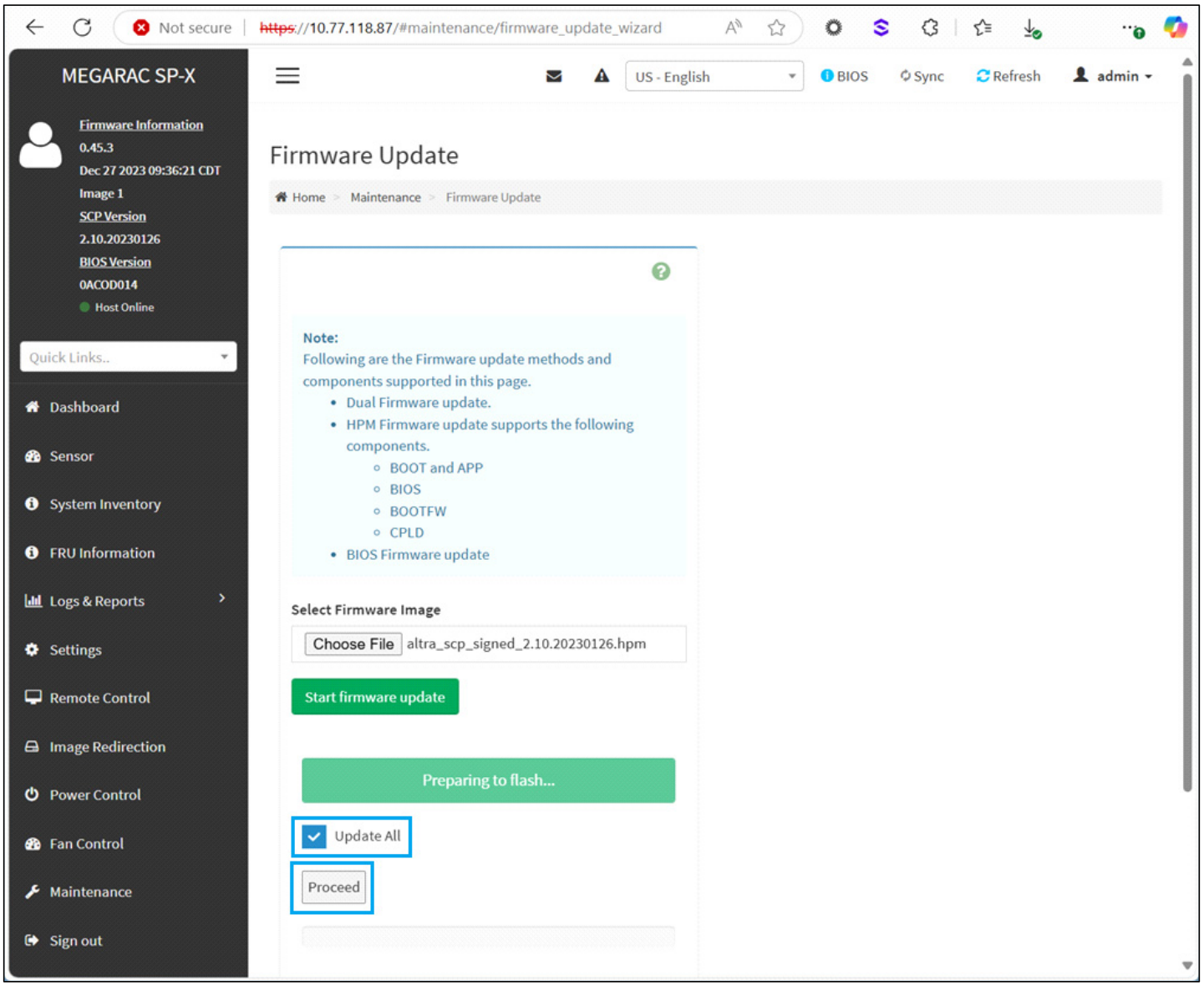
1. Launch a Web browser (such as Firefox or Chrome) and type **https://BMC_IP** in the address field to access the BMC WebUI.
   Note: The login ID for BMC is “admin”, and the login password is “admin”.
2. Click Maintenance > Firmware Update.



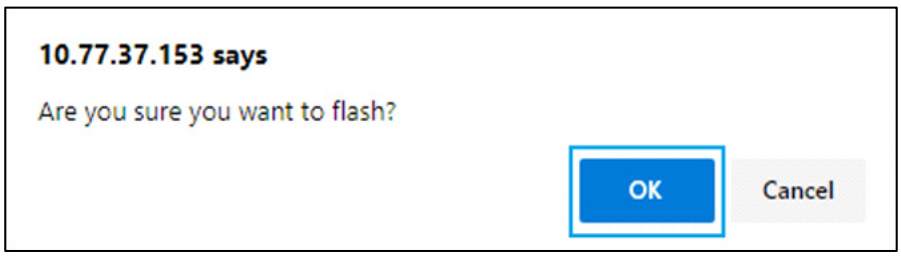
3. Click **Choose File**. Select the correct file with a ".hpm" extension (for example, `altra_scp_signed_2.10.20230126.hpm`) from the host and click **Start firmware update**.



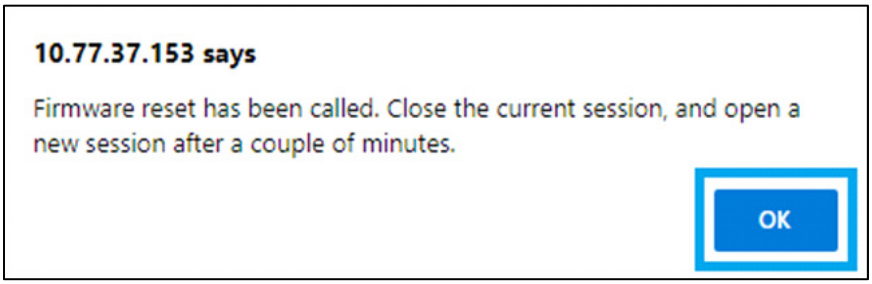
4. If the versions differ, click **Proceed** to start the upgrade.



5. Click **OK** to start the firmware upgrade process.



6. After the upgrade is complete, click OK to exit.

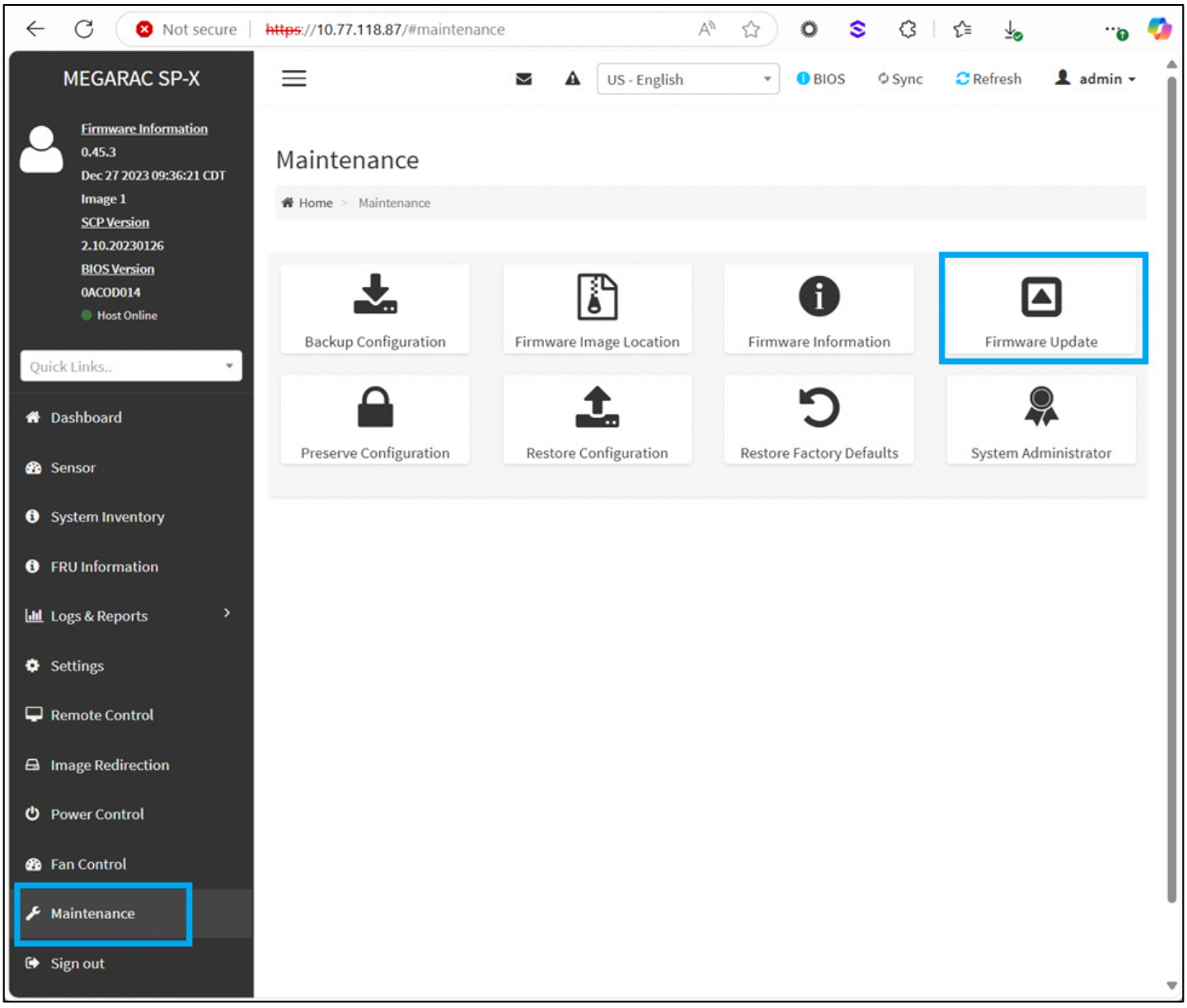


10. Step 6 — Upgrade UEFI Firmware

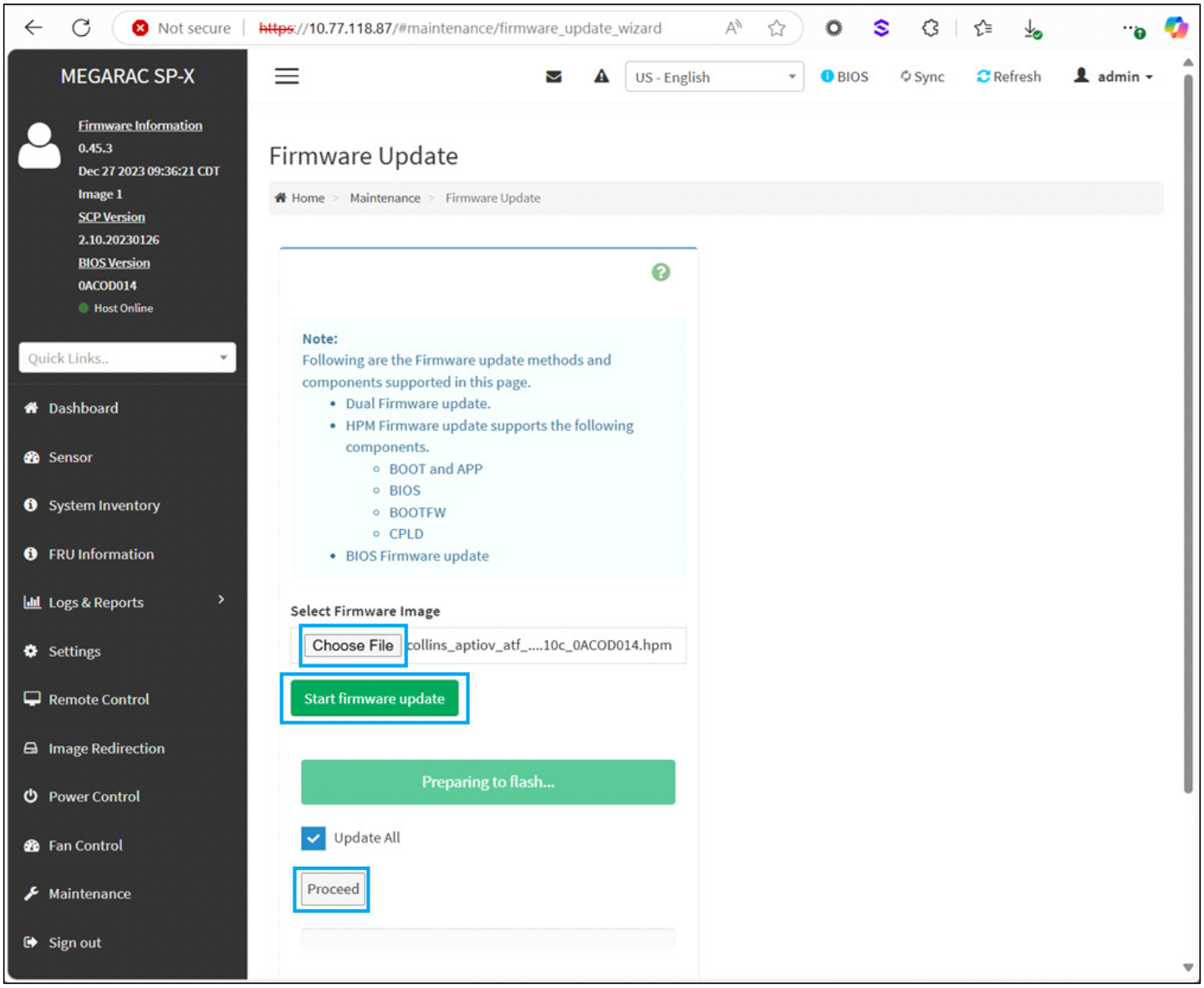
The UEFI firmware can be upgraded using either WebUI or IPMI as described in the following sections.

10.1. Step 6a — Upgrade UEFI Firmware Using WebUI

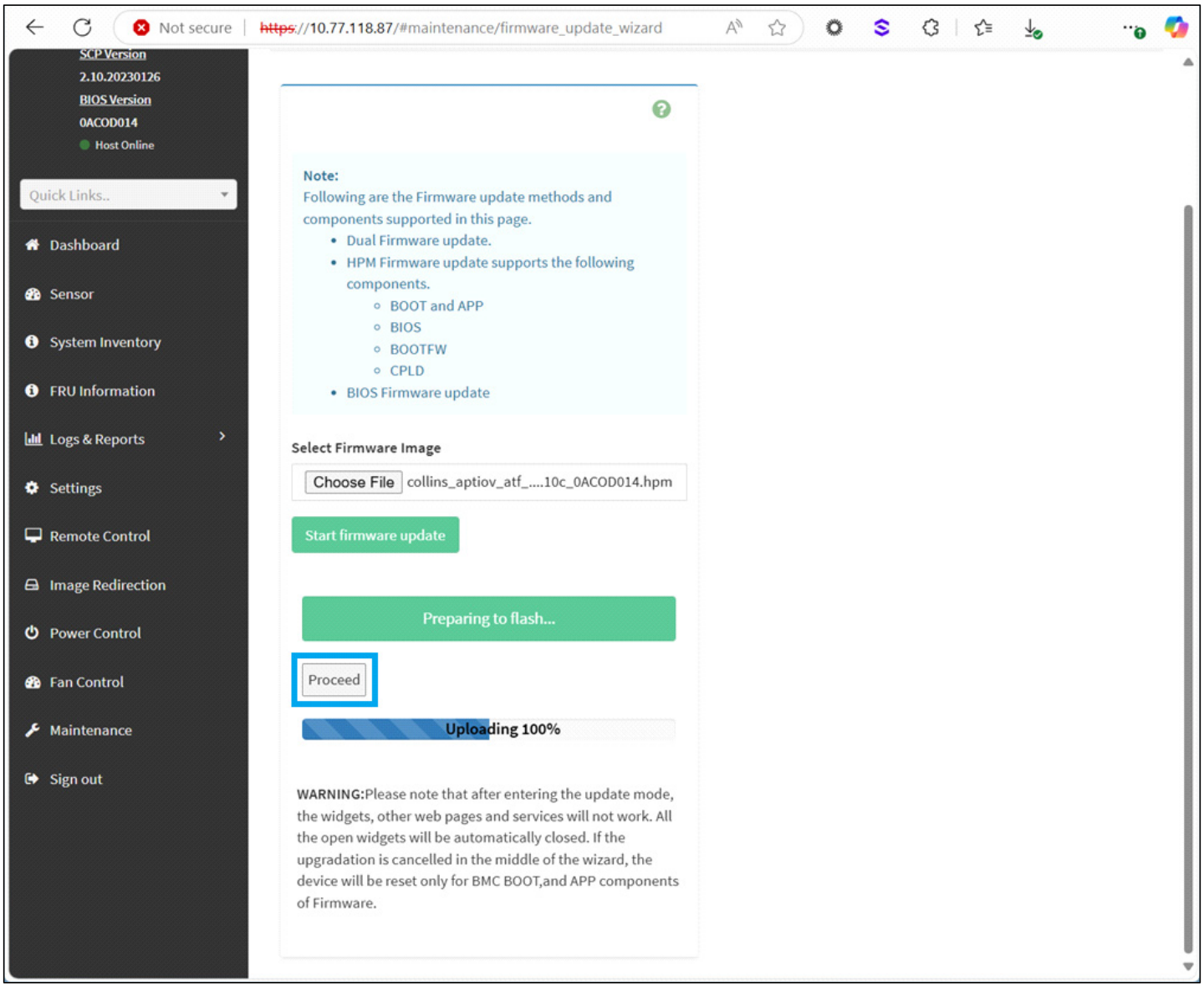
1. Launch a Web browser (such as Firefox or Chrome) and type **https://BMC_IP** in the address field to access the BMC WebUI.
   Note: The login ID for BMC is “admin”, and the login password is “admin”.
2. Click Maintenance > Firmware Update.



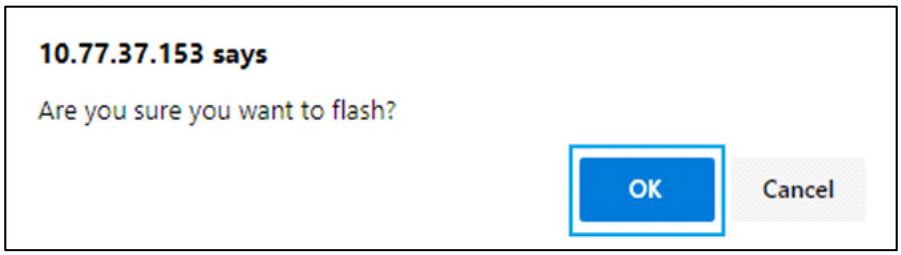
3. Click **Choose File**. Select the correct file with a ".hpm" extension (for example, `0ACOD014.hpm`) from the host and click **Start firmware update**.



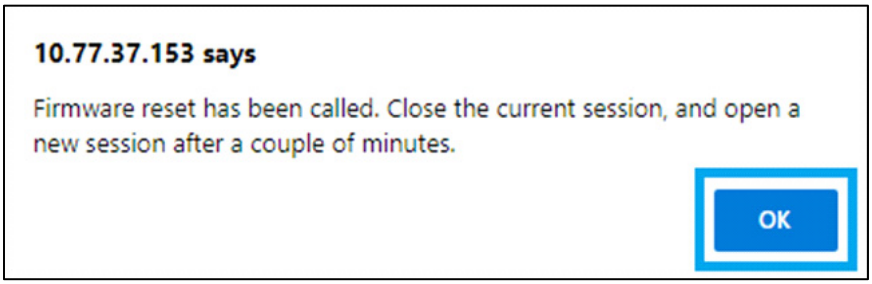
4. Click **Proceed**.



5. Click **OK** on the subsequent dialog box to start the firmware upgrade process.



6. After the upgrade is complete, click OK to exit.



11. Get the Most From the Documentation

The following list shows the Mt. Collins documentation that is available on the Ampere Computing secure website at https://connect.amperecomputing.com.

- Ampere Altra Platform Series Mt. Collins DVT/PVT/MP NVMe Getting Started Guide (this document)
- Altra Platform Hardware Design Specification
- Mt. Collins Schematics
- 2U Mt. Collins User's Guide

Additional Mt. Collins documentation is available in the firmware packages. Refer to *Appendix B: Mt. Collins Firmware Packages* for the firmware package contents.

11.1. Additional Resources

Additional collateral for the Ampere Altra Platform Series' processors, such as datasheet, user's manual, and software, are available on the Ampere Computing secure website at https://connect.amperecomputing.com.

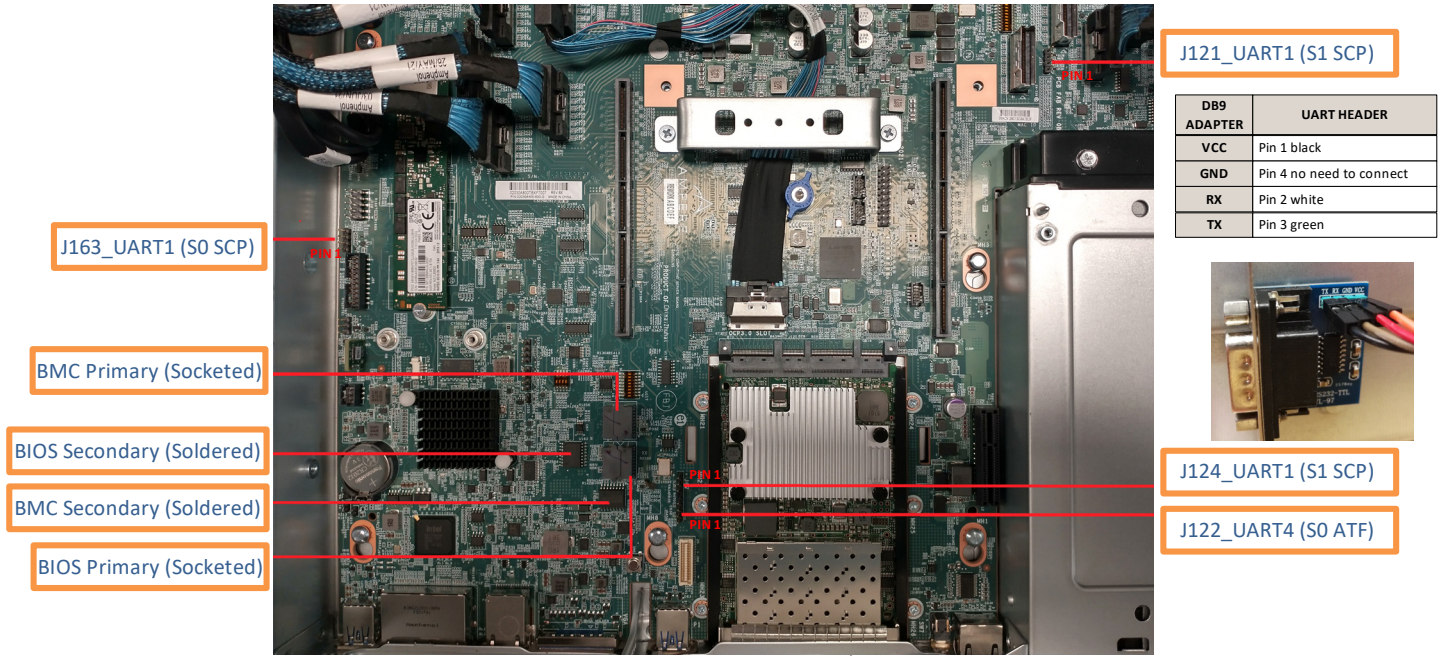
11.2. If You Need Help

For help with using the system, contact technical support at https://connect.amperecomputing.com/help.

12. Appendix A: BMC/BIOS SPI-NOR, SCP, and UART Locations

Figure 11 shows the locations of the BMC/BIOS SPI-NOR, SCP, and UART on the Mt. Collins motherboard.

Figure 11: BMC/BIOS SPI-NOR, SCP, and UART Locations on Mt. Collins Motherboard



DB9 ADAPTER	UART HEADER
VCC	Pin 1 black
GND	Pin 4 no need to connect
RX	Pin 2 white
TX	Pin 3 green

13. Appendix B: Mt. Collins Firmware Packages

13.1. Firmware Version for Altra/Altra Max Based Mt. Collins Server

The version numbering for the Altra/Altra Max based Mt. Collins firmware is in the format of 2.Xy, where X is the major release and y is the minor patch or bug fix on top of X.

As of this writing of this document, the latest firmware version available on the Ampere Customer Connect website at https://connect.amperecomputing.com is Software Release Package (SRP) 2.10c.

Following are the contents of the top-level firmware package:

```
Mt_Collins_SRP_2.10c_Binary Package_20231227
├── mt.collins-fw-aptv-bin-r2.10c-0ACOD014-20231219.tar.xz
├── mt.collins-fw-aptv-userdoc-r2.10c-0ACOD014-20231219.tar.xz
├── mt-collins-srp-mgmt-mgr-bin-r1.12-0.45_3.20231227.tar.xz
└── mt-collins-srp-mgmt-mgr-userdoc-r1.12-0.45_3.20231227.tar.xz
```

Following is the structure of the management firmware package:

```
mt-collins-srp-mgmt-mgr-bin-r1.12-0.45_3.20231227
├── amp_megarac_sdk
│   ├── bin
│   │   ├── BMC
│   │       ├── MtCollinsBmc0_45_3.hpm
│   │       ├── MtCollinsBmc0_45_3.ima
│   │       ├── README.txt
│   │   ├── CPLD_VRD
│   │       ├── CPLD
│   │       ├── Front Panel
│   │       ├── Mother Board
│   │       ├── Rear Panel
│   │           ├── For Altra
│   │               ├── MtCollins_12NVME_BP_CPLD_v06_20220408.hpm
│   │               ├── MtCollins_12NVME_BP_CPLD_v06_20220408.jed
│   │               ├── MtCollins_24SATA_HDDBP_CPLD_V02_20210303.hpm
│   │               ├── MtCollins_24SATA_HDDBP_CPLD_V02_20210303.jed
│   │           ├── For Altra Max
│   │               ├── MtCollins_12NVME_HDDBP_CPLD_V02_forAltraMaxCpu_20220630.hpm
│   │               ├── MtCollins_12NVME_HDDBP_CPLD_V02_forAltraMaxCpu_20220630.jed
│   │               ├── MtCollins_24NVME_HDDBP_CPLD_v02_forAltraMAXCpu_20220630.hpm
│   │               ├── MtCollins_24NVME_HDDBP_CPLD_v02_forAltraMAXCpu_20220630.jed
│   │           ├── MtCollins_12Hybrid_HDDBP_CPLD_PVT_v19_20220416.hpm
│   │           ├── MtCollins_12Hybrid_HDDBP_CPLD_PVT_v19_20220416.jed
│   │           ├── MtCollins_12SATA_HDDBP_CPLD_V1313_20220630.hpm
│   │           ├── MtCollins_12SATA_HDDBP_CPLD_V1313_20220630.jed
│   │           ├── MtCollins_24NVME_HDDBP_CPLD_v14_20220630.hpm
│   │           ├── MtCollins_24NVME_HDDBP_CPLD_v14_20220630.jed
```

```
|   |       ├── Mother Board
|   |       |     ├── Mt.Collins_MB_CPLD_v06_20220607.hpm
|   |       |     ├── Mt.Collins_MB_CPLD_v06_20220607.jed
|   |       ├── Rear Panel
|   |       |     ├── 2Rear_HDDBP_CPLD_PVT_V13_20220324.hpm
|   |       |     ├── 2Rear_HDDBP_CPLD_PVT_V13_20220324.jed
|   |   ├── VRD
|   |       ├── Foxconn_MtCollins_XDPE12284c_1n1_SOCnRCA__50F05078_20210412_144245.hpm
|   |       ├── Foxconn_MtCollins_XDPE12284c_1n1_SOCnRCA__50F05078_20210412_144245.xsf
|   |       ├── Foxconn_MtCollins_XDPE12284c_4n1_MEM__341F194C_20210412_144330.hpm
|   |       ├── Foxconn_MtCollins_XDPE12284c_4n1_MEM__341F194C_20210412_144330.xsf
|   |       ├── Foxconn_MtCollins_XDPE12284c_8n0_PCP_zero loadline_modifiedOCP_20220302_B5043919.hpm
|   |       ├── Foxconn_MtCollins_XDPE12284c_8n0_PCP_zero loadline_modifiedOCP_20220302_B5043919.xsf
|   |   ├── README.txt
|   |   ├── Upgrading failed with wrong CPLD firmware.png
|   |   ├── Upgrading success with right CPLD firmware.png
|   ├── checksum.txt
| docs
|   ├── BMC_Release_Note.txt
|   ├── MB_CPLD_Release Notes_20220607.txt
|   ├── SOP_BIOS_HPM_Out-Band.pdf
|   ├── SOP_BIOS_Out-Band_YafuFlash.pdf
|   ├── SOP_BIOS_WebUI_Flash.pdf
|   ├── SOP_BMC_HPM_Out-Band.pdf
|   ├── SOP_BMC_Out-Band_YafuFlash.pdf
|   ├── SOP_BMC_WebUI_Flash.pdf
|   ├── SOP_MB_CPLD_HPM_Out-Band.pdf
|   ├── SOP_MB_CPLD_Out-Band_YafuFlash.pdf
|   ├── SOP_MB_CPLD_WebUI_Flash.pdf
|   ├── SOP_SCP_Out-Band.pdf
|   ├── SOP_SCP_WebUI_Flash.pdf
|   ├── checksum.txt
| docs
|   ├── BMC_Release_Notes.txt
|   ├── MB_CPLD_Release_Notes_20210728.txt
|   ├── SOP_BIOS_HPM_Out-Band.pdf
|   ├── SOP_BIOS_Out-Band_YafuFlash.pdf
|   ├── SOP_BIOS_WebUI_Flash.pdf
|   ├── SOP_BMC_HPM_Out-Band.pdf
|   ├── SOP_BMC_Out-Band_YafuFlash.pdf
|   ├── SOP_BMC_WebUI_Flash.pdf
|   ├── SOP_MB_CPLD_HPM_Out-Band.pdf
```

```
│   ├── SOP_MB_CPLD_Out-Band_YafuFlash.pdf
│   ├── SOP_MB_CPLD_WebUI_Flash.pdf
│   ├── SOP_SCP_Out-Band.pdf
│   ├── SOP_SCP_WebUI_Flash.pdf
└── info
│   ├── Foxconn_BMC_User_Guide.pdf
│   ├── Foxconn_Redfish_User_Guide.pdf
│   ├── System_FW_Upgrade_Guide.txt
```

Following is the structure of the SCP and BIOS firmware package:

```
mt.collins-fw-aptv-bin-r2.10c-0ACOD014-20231219
└── altra_firmware_sdk
    ├── bin
    │   ├── aptiov
    │   │   ├── CapsuleApp.efi
    │   │   ├── checksum.txt
    │   │   ├── collins_aptiov_atf_signed_2.10c_0ACOD014.cap
    │   │   ├── collins_aptiov_atf_signed_2.10c_0ACOD014.hpm
    │   │   └── collins_aptiov_atf_signed_2.10c_0ACOD014.spi
    │   └── scp
    │       ├── altra_scp_signed_2.10.20230126.hpm
    │       └── altra_scp_signed_2.10.20230126.slim
    └── docs
        ├── Altra_Family_SCP_UM_v0.61_20220303.pdf
        ├── CHANGELOG.txt
        └── Mt.Collins-BIOS-0ACOD014-ReleaseNote.txt
```

14. Appendix C: Identifying Mt. Collins Motherboard Revisions

Table 15 lists the Mt. Collins versions along with the motherboard revisions used for each of them.

Table 15: Mt. Collins Version Mapped to Motherboard Revision

MT. COLLINS REVISION (EVT/DVT/PVT/MP)	MOTHERBOARD REVISION
DVT	BX
	DX
	EX
PVT	IX
	KX
MP	0B

Figure 12 shows the top view of the Mt. Collins motherboard with the Board Revision identifier label highlighted.

Figure 12: Top View of Mt. Collins Server Motherboard

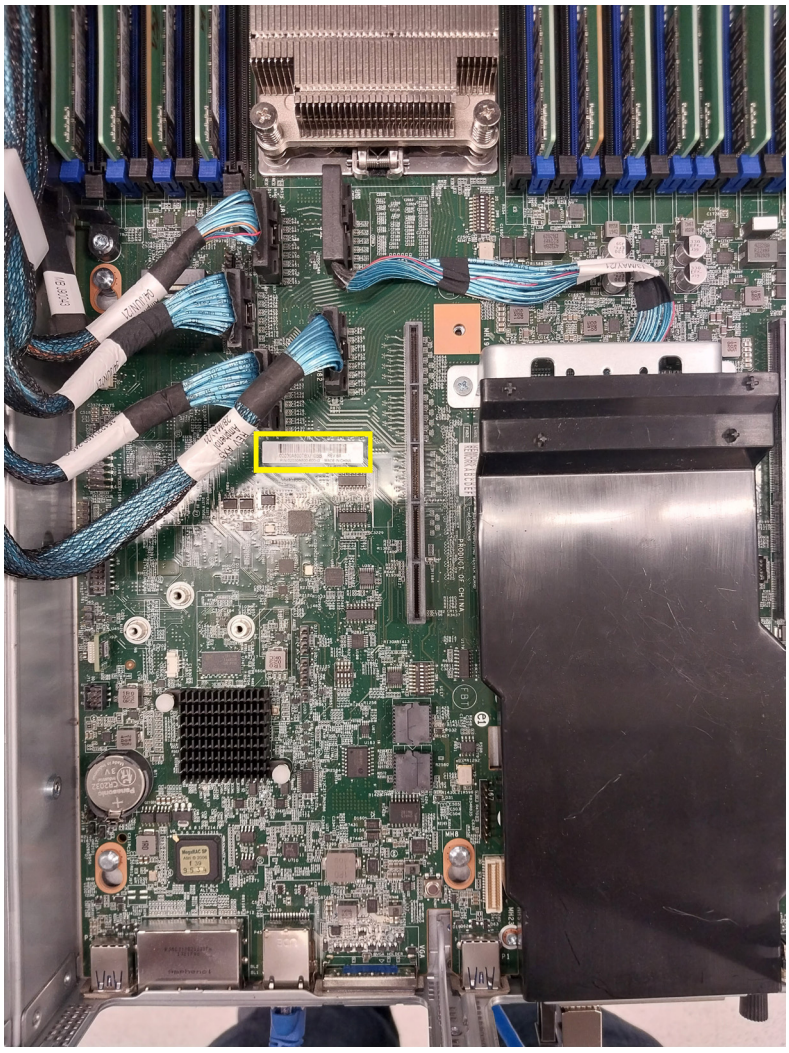
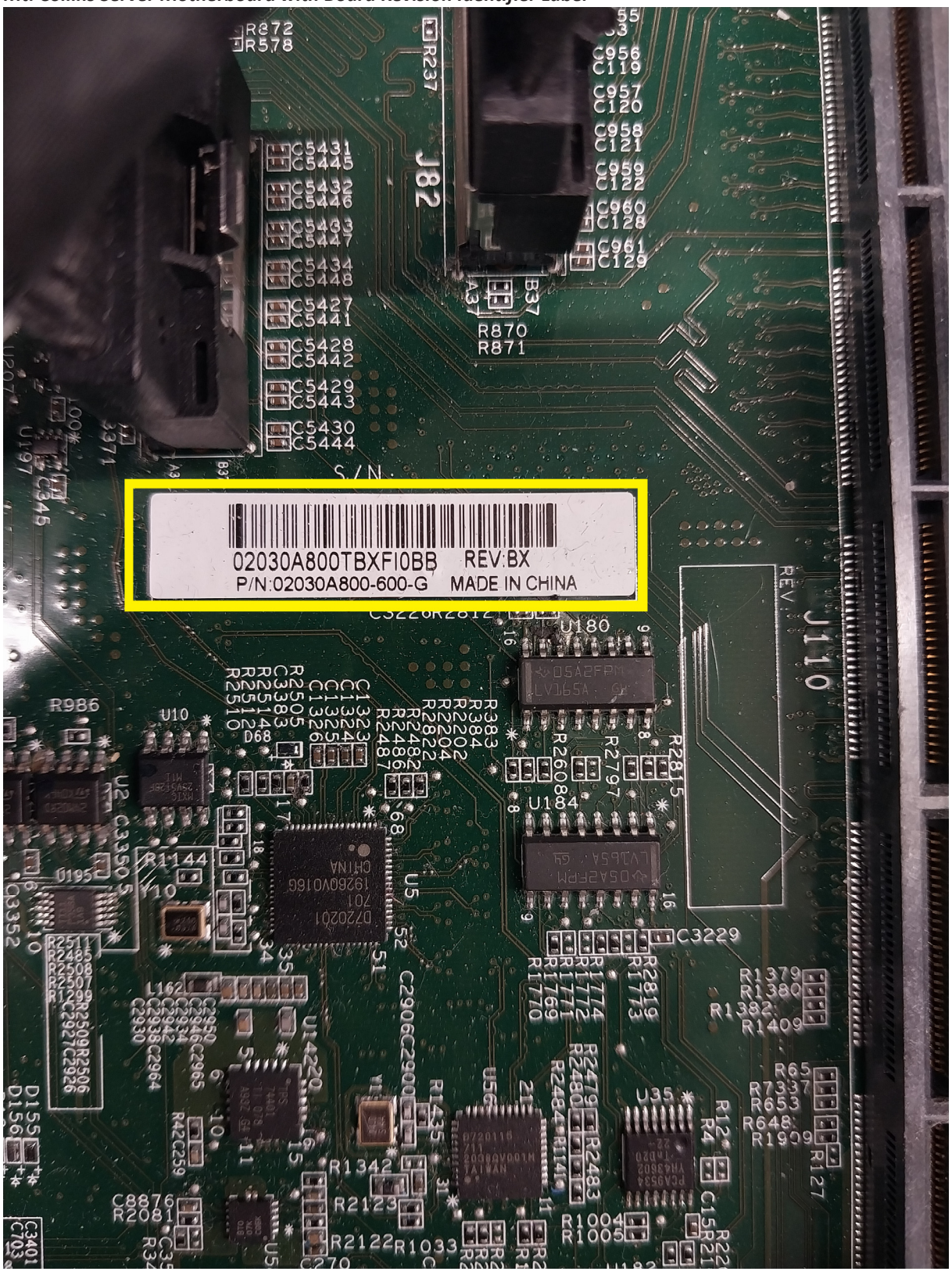


Figure 13 shows the details printed on the Board Revision identifier label.

Figure 13: Mt. Collins Server Motherboard with Board Revision Identifier Label



15. Revision History

ISSUE	DATE	DESCRIPTION
1.00	August 12, 2025	Updated the document for the Mt. Collins Mass Production (MP) SKU with SRP 2.10c.
0.85	March 29, 2024	Updated the following: • *Table 11, "Mt. Collins DDR4 Memory Population Table (Max 32 DIMM Slots)", on page 11* • *Table 12, "Mt. Collins DVT/PVT Server Supported Memory Channel Configurations – Socket0", on page 12*
0.80	November 8, 2023	Updated the following: • *Table 2, "Standard Shipping Configuration for Mt. Collins DVT Server", on page 1* • *Table 4, "Mt. Collins DVT/PVT Contents List", on page 3* • *Table 5, "Ports, Connectors, and Buttons on the Rear Side of the Mt. Collins Server", on page 4* • *Table 6, "Ports, Connectors, and Buttons on the Front Side of the Mt. Collins Server", on page 5* Added the following: • *Table 3, "Standard Shipping Configuration for Mt. Collins PVT/MPAppendix C: Identifying Mt. Collins Motherboard Revisions (page 35)* Minor fixes and corrections.
0.70	May 17, 2022	Initial release.

August 12, 2025

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